energies

MDPI

Article

Multivariable Unconstrained Pattern Search Method for Optimizing Digital PID Controllers Applied to Isolated Forward Converter

Ghulam Abbas [1,*], Muhammad Usman Asad [2,*], Jason Gu [2], Salem Alelyani [3,4], Valentina E. Balas [5,*], Mohammad Rashid Hussain [3,4], Umar Farooq [6], Ahmed Bilal Awan [7], Ali Raza [1] and Chunqi Chang [8]

1 Department of Electrical Engineering, The University of Lahore, Lahore 54000, Pakistan; ali.raza@ee.uol.edu.pk
2 Department of Electrical and Computer Engineering, Dalhousie University, Halifax, NS B3H 4R2, Canada; jason.gu@dal.ca
3 Center for Artificial Intelligence (CAI), King Khalid University, Abha 61421, Saudi Arabia; s.alelyani@kku.edu.sa (S.A.); humohammad@kku.edu.sa (M.R.H.)
4 College of Computer Science, King Khalid University, Abha 61421, Saudi Arabia
5 Department of Automatics and Applied Software, "Aurel Vlaicu" University of Arad, 310130 Arad, Romania
6 Department of Electrical Engineering, University of the Punjab, Lahore 54590, Pakistan; engr.umarfarooq@yahoo.com
7 Department of Electrical and Computer Engineering, College of Engineering and Information Technology, Ajman University, Ajman, UAE; a.awan@ajman.ac.ae
8 School of Biomedical Engineering, Health Science Center, Shenzhen University, Shenzhen 518060, China; cqchang@szu.edu.cn
* Correspondence: ghulam.abbas@ee.uol.edu.pk (G.A.); usmanasad01@hotmail.com (M.U.A.); valentina.balas@uav.ro (V.E.B.)

Citation: Abbas, G.; Asad, M.U.; Gu, J.; Alelyani, S.; Balas, V.E.; Rashid Hussain, M.; Farooq, U.; Awan, A.B.; Raza, A.; Chang, C. Multivariable Unconstrained Pattern Search Method for Optimizing Digital PID Controllers Applied to Isolated Forward Converter. *Energies* **2021**, *14*, 77. https://dx.doi.org/10.3390/en14010077

Received: 2 November 2020
Accepted: 21 December 2020
Published: 25 December 2020

Abstract: Most of the traditional PID tuning methods are heuristic in nature. The heuristic approach-based tuned PID controllers show only nominal performance. In addition, in the case of a digital redesign approach, mapping of the heuristically-designed continuous-time PID controllers into discrete-time PID controllers and in case of the direct digital design approach, mapping of the continuous-time plant (forward converter) into the discrete-time plant, results in frequency distortion (or warping). Besides this, nonlinear elements such as ADC and DAC, and delay in the digital control loop deteriorate the control performance. There is a need to tune conventionally-designed digital controllers to enhance performance. This paper proposes optimized discrete-time PID controllers for a forward DC–DC converter operating in continuous conduction mode (CCM). The considered conventional digital PID controllers designed on the basis of the digital redesign and direct digital approaches are tuned by one of the multivariable unconstrained pattern search methods named Hooke–Jeeves (H–J) search method to ensure excellent output voltage regulation performance against the changes in input voltage and load current. Numerical results show that the H–J-based optimized PID compensated forward converter system shows tremendous improvement in performance compared to its unoptimized counterpart and simulated annealing (SA)-based compensated system, thus justifying the applicability of the H–J method for enhancing the performance.

Keywords: discrete-time PID controller; Hooke–Jeeves algorithm; isolated forward converter; multivariable unconstrained pattern search method; simulated annealing

1. Introduction

Forward converters, which are popular switched-mode power supplies (SMPSs), have a simple circuit configuration, as they employ a single power transistor referenced to the primary-side return. Forward converter topologies (especially single-ended), typically used in off-line applications in the 100 W−300 W region, are extensively used in applications such as telecom central office equipment, smartphones, systems that use distributed power

architectures, and DC–DC applications in industrial controls [1]. These low to medium power conversion applications require a tightly-regulated output voltage.

Better load and line regulations are hard to achieve through an open-loop switching converter system. Analog compensators suffer from limitations such as low reliability and flexibility, large size, poor design portability, and so on. Although digital compensators are gaining the attention of control system designers and researchers due to their programmability, configurability, and ability to realize complex and sophisticated control approaches, they suffer from nonlinear effects, such as ADC and DAC quantization errors, sampling and hold effects, loop delay, and so on, which deteriorate the performance by limiting the loop bandwidth. Digital controller performance can be enhanced by tuning their coefficients (after ones designed traditionally) using an optimization technique. This paper proposes the gradient-free Hooke–Jeeves pattern search method for optimizing discrete-time Proportional–Integral–Derivative (PID) compensators applied to an isolated forward DC–DC converter.

2. Literature Review

Regarding the literature review, in [2], a dual-loop control strategy, where an analog PI controller was used for the synthesis of both the internal current control loop and the external voltage control loop, was proposed for a galvanically isolated forward converter to ensure better transient response and reduced ripples in the output voltage. For both the loops, the PI controller was designed based on crossover frequency and phase margin characteristics. In [3], an output current-differential (OCD) control scheme having a master–slave structure was proposed for a three forward converters-based input-series–output-parallel (ISOP) system. The output voltage regulator (OVR) loop designed for a master module (to provide current references to slave modules) and individual load–current sharing loops developed for slave modules (to regulate the current in each module equally) of the OCD control scheme were constructed using the frequency–response characteristics. In [4], the authors, however, proposed a digital PI controller implemented through Digital Signal Processor (DSP) for OVR and input voltage sharing (IVS) for a modular ISOP system. Various analog compensators, including PI, PID, and lead were designed heuristically and applied to forward converter to ensure better control performance [5]. In [6], regulation of the most effective DC output voltage of a multiple output high frequency (MOHF) isolated forward converter mainly designed for power factor correction (PFC) was achieved by the heuristic Ziegler Nichols method-based tuned PI controller. In [7], for a single-ended forward circuit, negative feedback for driving MOSFET was accomplished through an operational amplifier (from Texas Instruments) with high-bandwidth. The control loops (mostly analog in nature) suggested in all the references mentioned above for switching converters are designed based on classical control theory. There occurs usually a tradeoff between robustness and transient response in such types of controllers.

To overcome the limitations, recently other artificial intelligence and nonlinear control theory-based control techniques have also been reported in the literature. Authors in [8] suggested a fuzzy-neural sliding-mode controller (FNSMC) comprising a neural controller and a compensation controller for a PWM-based isolated forward converter to achieve excellent load and line regulations. Authors in [9] concluded through simulation results that the fuzzy PID controller displayed better transient and steady-state performance than did PID and fuzzy controllers when applied to push–pull forward (PPF) DC–DC converter. In [10], two controllers, called a self-regulating fuzzy logic control (SR-FLC) and a fuzzy sliding-mode control (SR-FSMC) were proposed for a forward DC–DC converter. To avoid a time-consuming trial-and-error tuning procedure, fuzzy rules were adjusted by a gradient-based rule modifier. A fuzzy logic controller (FLC) along with PI was successfully developed and applied to a modular forward converter-based input-parallel–output-series (IPOS) system [11] and a forward converter with an active clamp circuit (ACFC) [12] used in the telecom power supply. In [13], the fuzzy logic-based PI controller was suggested for a bidirectional dual active bridge converter. In [14], a sliding mode

controller was applied to a forward converter to achieve regulated output voltage even against load transients. An adaptive disturbance observer (ADO)-based practical terminal sliding mode control (TSMC) that required no exact feedback linearization about the plant dynamics was suggested in [15]. The ADO-TSMC guaranteed high control accuracy and rapid convergence by adopting a TSMC-type surface. In [16], the adaptive nonsingular TSMC was integrated with neural networks (NNs) to realize fault-tolerant control for the simultaneous compensation of model uncertainties and disturbances, as well as actuator faults. Authors in [17] proposed a robust PID controller with quantitative feedback theory (QFT) to ensure stability in the presence of model uncertainties and external disturbances. The control approaches, however, may require a time-consuming trial-and-error tuning procedure to ensure superior performance.

Owing to rapid advances in digital control technology, researchers have also suggested digital control loops for isolated DC–DC converters. In [18], for a central-tapped full-bridge converter to display superior line regulation, the two dedicated control loops were realized using a digital PID compensator. An FPGA-based on-line tuned PID controller was also suggested in [19] for a forward converter to attain better control performance without pin-pointing the procedure of calculating PID parameters. A conventionally designed analog PID controller for a specific bandwidth (crossover frequency), and phase margin was digitally implemented by DSP to regulate the output voltage of a full-bridge active-clamp forward-flyback (FBACFF) converter in [20]. Only a notion of the microcontroller-based implementation of digital control for a forward converter with a DC electromagnet as a load of an SMPS designed for electromagnet systems was given in [21] to keep output voltage regulated against the input voltage sag.

Limited research has been carried out on realizing digital controllers for isolated switching converters. Digital control loop nonlinearities, warping (or distortion) in digital frequency response during (approximate) mapping from s-plane into z-plane, and so on have detrimental effects on digital controller performance. Proper retuning of once traditionally designed digital PID controllers by optimization techniques may diminish nonlinear effects to obtain the required transient response. The gradient-free H–J method is employed here for retuning controller coefficients. The method uses flexible searching steps to ensure the near-optimal solution and offers characteristics such as simplicity, robustness, and versatility. This methodical pattern search technique yields an optimum solution for an effectively-distinct cost (objective) function and handles well, especially for small- and medium-sized optimization problems. This lays a good foundation for the construction of this paper.

Additionally, the H–J method is deterministic, as it does not involve randomness during its progression. It converges to the same end solution on every run for the same initial point. On the other hand, a metaheuristic optimization method converges to a different point every time it is executed. The process may sometimes become laborious for finding the best solution in the case of metaheuristics. Once compared to one of the metaheuristics, such as simulated annealing (in our case), the H–J method gives promising results and shows an optimal end solution. This justifies the applicability of the H–J method to the optimized digital control algorithms applied to the forward converter.

The paper is structured in the following way. Section 2 presents the literature review of the state-of-the-art. Section 3 describes the dynamics (i.e., the transfer function) of a forward DC–DC converter required for the design of discrete-time PID controllers. The design of four types of discrete-time PID controllers based on classical control theory is presented in Section 4. The H–J search algorithm employed for optimizing digital PID controllers is described in detail in Section 5. Simulation results are presented in Section 6. Hardware into the loop implementation is pinpointed in Section 7. Finally, conclusions are drawn in Section 8.

3. Description of Forward Converter Dynamics

For the sake of designing the required control loop, the transfer function (dynamics) of a forward DC–DC converter should be known. A simplified schematic of a forward DC–DC converter is shown in Figure 1. It consists of a controllable switch Q (MOSFET, BJT, IGBT, and so on), a three-winding isolation transformer with a demagnetizing (reset) winding, diodes D_1, D_2, and D_3, an output filter inductor L with its direct current resistance (DCR) r_L, an output filter capacitor C with its equivalent series resistance (ESR) r_C, and a load resistance R. Bifilar transformer winding with ratio 1:1 for N_p:N_r is normally used. The auxiliary (reset) winding helps in resetting the transformer during the switching off period to avoid core saturation.

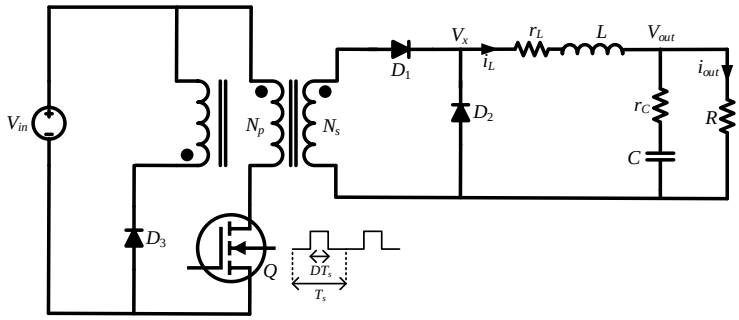


Figure 1. Circuit diagram of a forward DC–DC converter with reset winding.

Consider the converter working in CCM in two modes, as shown in Figure 2. When transistor Q switches are on, primary current i_p rises linearly from zero; diode D_2 becomes reverse-biased; voltage V_{in} develops across primary winding N_{p}; energy is transferred from the primary winding to the secondary and then through the forward-biased D_1 to the L-C filter and load R. When transistor Q switches off, the transformer voltage gets reversed; diode D_1 gets reverse-biased, whereas diodes D_2 and D_3 become forward-biased; the primary reset winding with D_3 provides a path to the transformer magnetizing current to avoid core saturation; this forces the maximum duty cycle D_{max} not to exceed 50% theoretically for resetting transformer fully.

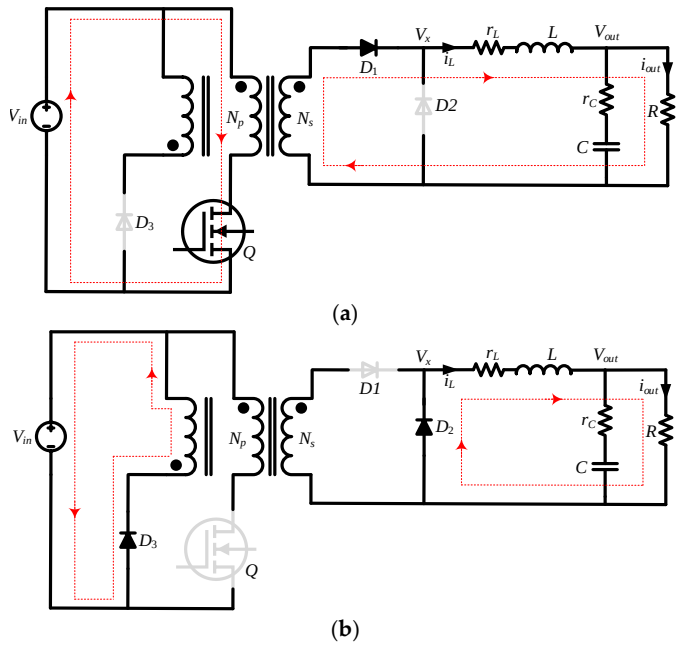


Figure 2. Equivalent circuit of the forward converter when transistor (**a**) switches on and (**b**) switches off.

The circuit element values taken for the forward converter design example, unless otherwise specified, are V_{in} = 36 V, V_{out} = 12 V, $n = N_s/N_p$ = 32/48, L_m = 10 mH, L = 400 µH, r_L = 120 mΩ, C = 100 µF, r_C = 33 mΩ, R = 10 Ω, and f_s = 60 kHz ($T_s = 1.67 \times 10^{-5}$ s).

Applying the inductor volt-second balance (IVSB) principle while neglecting all the losses, the DC transfer function of a forward converter can be expressed by

$$V_{out} = D\left(\frac{N_s}{N_p}V_{in}\right) = D(nV_{in}) \tag{1}$$

where $n\ (= N_s/N_p)$ represents the turn ratio of the transformer, and D is the duty ratio. The output–input voltage relationship of buck converter $V_{out} = DV_{in}$ becomes translated into the forward converter's $V_{out} = DnV_{in}$ if we replace V_{in} by nV_{in}.

Since the forward converter is a buck-derived isolated converter, its transfer function can be easily derived from the buck converter [22]. The well-established state–space averaging and linearization technique proposed by Middlebrook et al. [23] was employed to derive the buck converter's transfer function. The buck converter's transfer function can be translated into the forward converter's just by replacing V_{in} with nV_{in}, as already remarked. As a result, the control-to-output (or duty ratio-to-output) small-signal transfer function in the s-domain of the forward converter is expressed as

$$\begin{aligned} T_p(s) &= \left.\frac{\hat{v}_{out}(s)}{\hat{d}(s)}\right| \begin{matrix} \hat{v}_{in}(s) = 0 \\ \hat{i}_{out}(s) = 0 \end{matrix} \\ &= \frac{\left(\frac{N_s}{N_p}V_{in}\right)}{\left(1+\frac{r_L}{R}\right)}\left[\frac{(r_C Cs+1)}{LC\left(\frac{R+r_C}{R+r_L}\right)s^2+\left(\frac{L}{R+r_L}+C\left(\frac{Rr_L}{R+r_L}\right)+r_C C\right)s+1}\right] \\ &= \frac{\left(\frac{N_s}{N_p}V_{in}\right)}{\left(1+\frac{r_L}{R}\right)}\left(\frac{\frac{s}{\omega_{ESR}}+1}{\frac{s^2}{{\omega_0}^2}+\frac{s}{Q\omega_0}+1}\right) \end{aligned} \tag{2}$$

where

$$\omega_{ESR} = \frac{1}{r_C C} \tag{3}$$

$$\omega_0 = \frac{1}{\tau} = \frac{1}{\sqrt{LC\frac{R+r_C}{R+r_L}}} = \frac{1}{\sqrt{LC}}\sqrt{\frac{R+r_L}{R+r_C}} \tag{4}$$

$$Q = \frac{1}{2\zeta} = \frac{1}{\omega_0\left(\frac{L}{R+r_L}+C\left(\frac{Rr_L}{R+r_L}\right)+r_C C\right)} \tag{5}$$

Here ω_{ESR}, $\omega_0 = 1/\tau$, and $Q = 1/2\zeta$ signify the capacitor zero frequency, the filter resonance frequency, and the filter quality factor, respectively. From $T_p(s)$, it is observed that due to the presence of capacitor ESR, a zero frequency is introduced at $1/r_C C$ [24].

A pair of complex conjugate poles at ω_0 causes phase reduction, thus resulting in a low phase margin. For the component values mentioned above, the open-loop forward converter offers only a phase margin of 8.01° at 2.5×10^4 rad/s (see Figure 3). The low phase margin needs to be raised to achieve better transient and steady-state characteristics. This is accomplished by introducing a compensator into the loop, which introduces phase at the required crossover frequency to meet the required specifications.

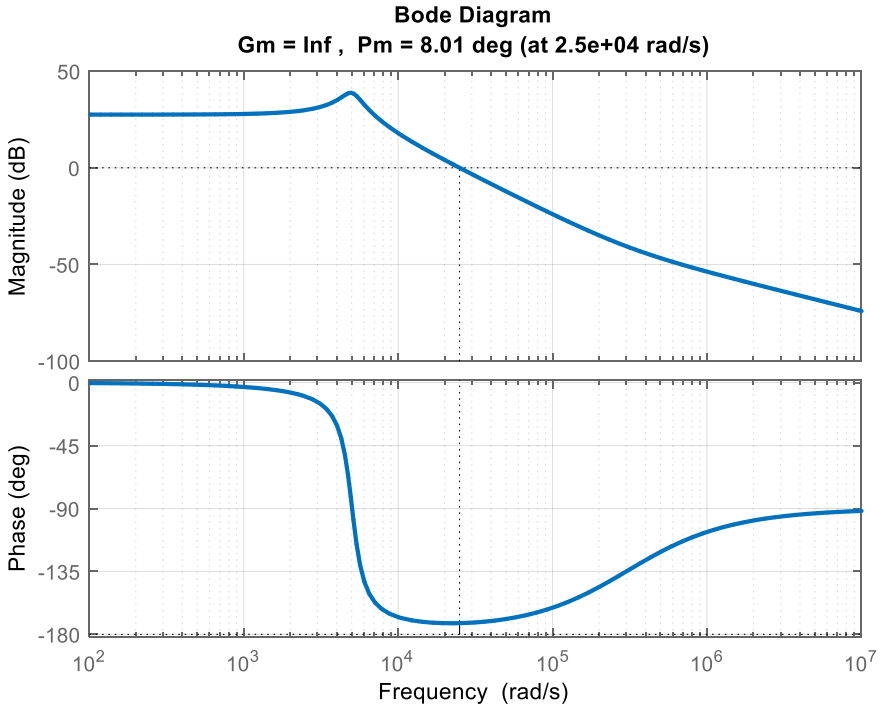


Figure 3. Bode plot of the open-loop forward converter.

For the digital compensated system, the analog plant has to be discretized. The continuous-time forward DC–DC converter $T_p(s)$ (plant) is discretized using zero-order-hold (ZOH) with $T_s = 1/(60 \times 10^3)$ s. That is to say,

$$T_p(z) = Z\left\{\frac{1-e^{-sT_s}}{s}.T_p(s)\right\} = \left(1-z^{-1}\right).Z\left\{\frac{T_p(s)}{s}\right\} \tag{6}$$

Using the values of the components mentioned above, the discretized plant by ZOH, numerically, can be expressed by

$$T_p(z) = \frac{0.1149z + 0.04927}{z^2 - 1.97z + 0.9773} \tag{7}$$

or

$$T_p(z) = \frac{0.1149z + 0.04927}{z^2 - 2\zeta_d w_d z + {w_d}^2} \tag{8}$$

with

$$\omega_d = e^{-\zeta\omega_0 T_s}, \quad \zeta_d = \cos\left(\omega_0 T_s\sqrt{1-\zeta^2}\right) \tag{9}$$

4. Conventional Digital Controller Design

Both the digital redesign or emulation and direct digital approaches are adopted in the paper to construct digital PID controllers. The first three PID controllers considered in the paper are first designed in s-plane for a specific phase margin and crossover frequency (frequency–domain characteristics). The analog PID controllers are then mapped into the digital PID controllers using different transformation techniques. The fourth PID controller is directly constructed in the z-plane for the discretized plant. In the case of switching converters, usually a compensator designed for a phase margin (PM) of 60° and 0-dB crossover frequency (ω_x) of one-tenth the converter switching frequency (f_s) guarantees acceptable rise and settling times, overshoots, and null steady-state error [14]. Unless otherwise specified, all considered PID compensators are designed for PM $\geq$ 60 ° and $\omega_x = \omega_s/10$.

It is worth mentioning that we employed four digital controllers to a forward converter. However, other approaches such as the PID-like coefficient diagram method (CDM) [25], one-degree-of-freedom (1DOF) [26] and 2DOF [27] PID, PID with derivative on output (DOO) [24], deadbeat control [28], and so on can also be utilized to realize controllers.

The digital closed-loop forward converter system is shown in Figure 4. The voltage error signal sampled by ADC is processed by a digital PID controller whose output (digital control signal), after its conversion into analog form, is fed to an analog forward converter. Conventionally-designed digital PID controllers are optimized by the H–J method. To facilitate the controller design, ADC, DAC, and delay gains are set to unity initially.

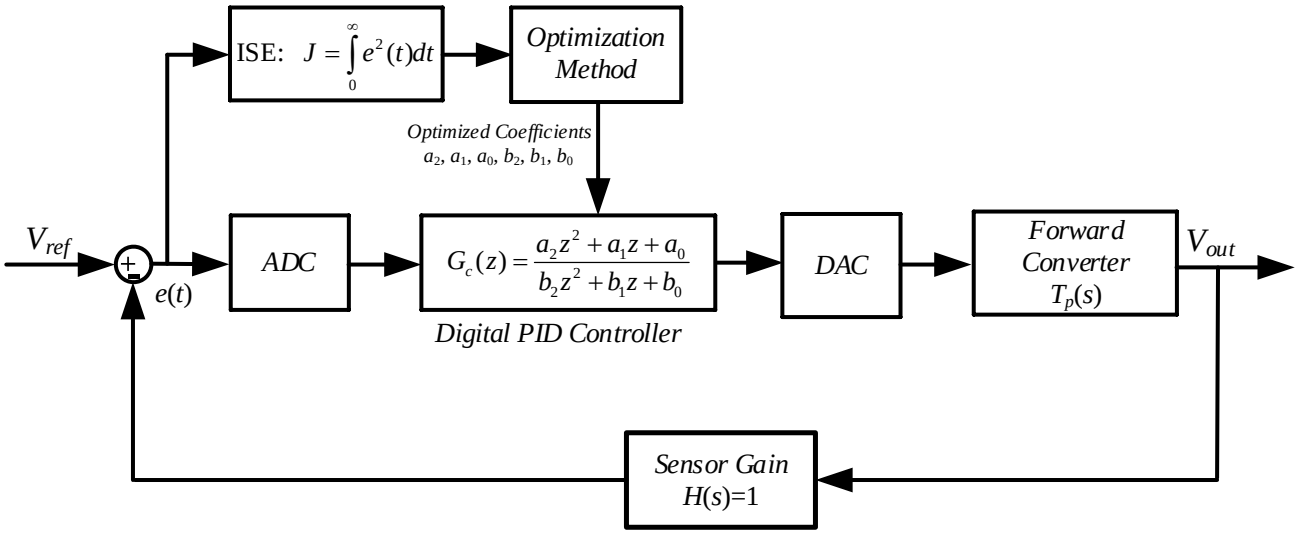


Figure 4. Forward converter digital control loop.

4.1. PID Controller with Complex Zeros

Open-loop complex poles of the forward DC–DC converter emerging due to an output LC filter should be damped as they cause phase reduction. The two complex poles can be compensated by two complex zeros of the compensator. The transfer function of the compensator in s-plane having two complex zeros ω_z at the LC resonant frequency ω_0 (i.e., $\omega_z = \omega_0$) to provide the necessary phase lead and an integrator to reduce steady-state error is expressed by

$$G_c(s) = K_c \frac{\left(\frac{s^2}{{\omega_z}^2} + \frac{s}{Q_C\omega_z} + 1\right)}{s} \tag{10}$$

Using $s = j\omega$, the magnitude and phase of $G_c(s)$ can be written as

$$\begin{aligned} |G_c(j\omega)| &= K_c\sqrt{\frac{(1-\omega^2/{\omega_z}^2)^2}{\omega^2} + \left(\frac{1}{Q_C\omega_z}\right)^2} \\ \angle G_c(j\omega) &= \begin{cases} -\tan^{-1}\left(Q_C\frac{-\omega^2+{\omega_z}^2}{\omega\omega_z}\right), \omega \le \omega_z \\ \tan^{-1}\left(Q_C\frac{\omega^2-{\omega_z}^2}{\omega\omega_z}\right), \omega > \omega_z \end{cases} \end{aligned} \tag{11}$$

For the complex conjugate zeros, the controller transfer function in (10) can also equivalently be written as

$$\begin{aligned} G_c(s) &= \frac{K_c}{{\omega_z}^2}\frac{\left(s^2+\frac{\omega_z s}{Q_C}+{\omega_z}^2\right)}{s} \\ &= \frac{K_c}{s{\omega_z}^2}(s+\alpha+j\beta)(s+\alpha-j\beta) \end{aligned} \tag{12}$$

where the pair of compensator complex zeros occurs at $s = -\alpha \pm j\beta$. The parameters α and β in terms of ω_z and Q_C can be written as

$$\begin{aligned} \alpha &= \tfrac{\omega_z}{2Q_C} = \tfrac{\pi f_z}{Q_C} \\ \beta &= \omega_z\sqrt{1-\tfrac{1}{4{Q_C}^2}} = 2\pi f_z\sqrt{1-\tfrac{1}{4{Q_C}^2}} \quad \text{with} \quad Q_C > 0.5 \end{aligned} \tag{13}$$

The compensator quality factor Q_C is set almost equal to the forward converter Q at maximum output current. The required DC gain K_c representing the PID integral gain is computed for the required $\omega_x = \omega_s/10$ by assuming that the control loop is compensated so the gain plot crosses 0 dB at a–1 slope, i.e.,

$$\begin{aligned} & T_p(s)\big|_{s=s_x}.\,G_c(s)\big|_{s=s_x} = 1 \\ \Rightarrow K_c &= \left.\frac{s}{\left(\frac{s^2}{{\omega_z}^2}+\frac{s}{Q_C\omega_z}+1\right)}\right|_{s=s_x}.\frac{1}{T_p(s)\big|_{s=s_x}} \end{aligned} \tag{14}$$

As all the parameters α, β, K_c, Q_C, etc. are known now, the transfer function of the analog controller numerically is calculated to be

$$G_c(s) = 6.2557\times 10^{-5}\left(\frac{s^2+1379s+2.522\times 10^7}{s}\right) \tag{15}$$

The above compensator is essentially a single-pole, two-zero compensator.

Various transformation techniques can be employed to map the analog PID compensator into its equivalent digital counterpart. We start with the simple mapping $z = e^{sT_s}$. The digital PID controller in its velocity form, one of the z-domain counterparts of the s-domain PID controllers, is generally given by

$$G_{MAP}(z) = \frac{U(z)}{E(z)} = K_{cz}\frac{z^2+k_1z+k_2}{z(z-1)} \tag{16}$$

Or equivalently, in discrete-time difference equation, the controller can be written as

$$u[n] = u[n-1] + K_{cz}(e[n] + k_1e[n-1] + k_2e[n-2]) \tag{17}$$

where K_{cz} is the gain of the discrete compensator.

The s-plane zeros s_1 and s_2 can be mapped to the corresponding z-plane locations z_1 and z_2 through $z_1 = e^{s_1T_s}$ and $z_2 = e^{s_2T_s}$, respectively [29]. If the complex zeros $z_1 = e^{-\alpha T_s + j\beta T_s}$ and $z_2 = e^{-\alpha T_s - j\beta T_s}$ (assuming that both the zeros lie in the same position) are the roots of the polynomial, then

$$\begin{aligned} & (z-z_1)(z-z_2) = 0 \Rightarrow z^2-(z_1+z_2)z+z_1z_2 = 0 \\ & \Rightarrow z^2 - 2e^{-\alpha T_s}\underbrace{\left(\frac{e^{j\beta T_s}+e^{-j\beta T_s}}{2}\right)}_{\cos(\beta T_s)}z + e^{-2\alpha T_s} = 0 \\ & \Rightarrow z^2 - 2r\cos\theta z + r^2 = 0 \\ & \text{where} \quad r = e^{-\frac{\pi f_z T_s}{Q_C}}; \quad \theta = 2\pi f_z T_s\sqrt{1-\tfrac{1}{4{Q_C}^2}}; \\ & \therefore z^2 + k_1z + k_2 = 0 \end{aligned} \tag{18}$$

with

$$\begin{aligned} k_1 &= -2r\cos\theta \\ k_2 &= r^2 \end{aligned} \tag{19}$$

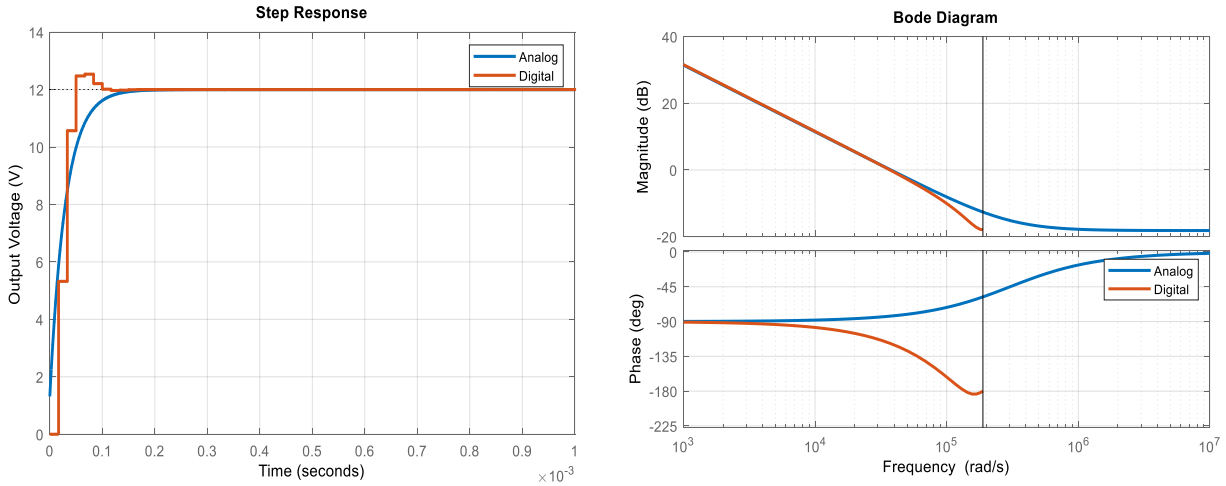
The other unknown parameter, the gain K_{cz} of the discrete-time PID compensator, can be computed by meeting the condition that $G_c(s)$ and $G_{MAP}(z)$ have the same magnitude at the desired loop crossover frequency f_x. That is to say,

$$\begin{aligned} G_{MAP}(z)|_{z=z_x=e^{j2\pi f_x T_s}} &= G_c(s)|_{s=s_x=j2\pi f_x} \\ \Rightarrow K_{cz} &= \frac{z(z-1)}{z^2+k_1 z+k_2}.G_c(s)|_{s=s_x} \end{aligned} \tag{20}$$

Performing some algebraic manipulations gives the digital controller as

$$\begin{aligned} G_{MAP}(z) &= 3.862\frac{z^2-1.97z+0.977}{z^2-z} \\ &= \frac{3.862z^2-7.610z+3.774}{z^2-z} \end{aligned} \tag{21}$$

From the step response and Bode plot shown in Figure 5, it can be noticed that the performance of the digital controller deteriorates slightly compared to its analog counterpart.



(**a**) (**b**)

Figure 5. (**a**) Output voltage response. (**b**) Bode plot for the open-loop compensated converter.

4.2. PID Controller with Real Zeros

The effect of converter complex poles causing phase reduction can also be nullified using compensator real zeros. For such a case, the analog PID controller with real zeros can be written as

$$G_c(s) = K_c\frac{\left(\frac{s}{\omega_{z1}}+1\right)\left(\frac{s}{\omega_{z2}}+1\right)}{s} \tag{22}$$

Here one of the real zeros is placed at ω_0 and the other slightly below ω_0 to provide the necessary phase lead. Keeping in view the converter power stage parameters, their position, however, can be adjusted differently in the vicinity of ω_0.

The DC gain K_c is computed to achieve the desired f_x by meeting the following condition:

$$K_c = \left.\frac{s}{\left(\frac{s}{\omega_{z1}}+1\right)\left(\frac{s}{\omega_{z2}}+1\right)}\right|_{s=s_x}.\frac{1}{T_p(s)|_{s=s_x}} \tag{23}$$

This gives the following analog controller as

$$G_c(s) = 6.0608\times10^{-5}\frac{(s+5022)(s+4017)}{s} \tag{24}$$

The compensator in (22) is of type interacting or series where the parameters K_c, ω_{z1}, and ω_{z2} are independent of one another. Equivalently, the PID controller having a noninteracting or parallel form with independent gains is given by

$$G_{PID}(s) = K_p + \frac{K_i}{s} + K_d s \tag{25}$$

The parameters of the noninteracting form can be derived from that of the interacting form and are related by the following expression:

$$\begin{aligned} K_p &= K_c\left(\tfrac{1}{\omega_{z1}} + \tfrac{1}{\omega_{z2}}\right) \\ K_i &= K_c \\ K_d &= \tfrac{K_c}{\omega_{z1}\omega_{z2}} \end{aligned} \tag{26}$$

The backward Euler transformation method with sampling time T_s is employed to map the parallel form of analog PID into its digital counterpart. This is accomplished by

$$G_{EULER}(z) = \left(K_p + \frac{K_i}{s} + K_d s\right)\Big|_{s=\frac{z-1}{zT_s}}$$

The above expression leads to the following discrete-time PID compensator.

$$G_{EULER}(z) = \frac{\left(K_d + K_p T_s + K_i T_s^2\right)z^2 - \left(2K_d + K_p T_s\right)z + K_d}{(z^2 - z)T_s} \tag{27}$$

Knowing all the compensator gains and sampling time, the discrete-time PID compensator is given by

$$G_c(z) = \frac{13.77z^2 - 25.75z + 12.29}{z^2 - 0.8488z - 0.1512} \tag{28}$$

Just like the case of complex zeros, the s-plane real zeros s_1 and s_2 of an analog PID controller can also be mapped into the corresponding z-domain zeros using $z_1 = e^{-\omega_{z1}T_s}$ and $z_2 = e^{-\omega_{z2}T_s}$, respectively. This implies

$$\begin{aligned} &z^2 - \left(e^{-\omega_{z1}T_s} + e^{-\omega_{z2}T_s}\right)z + e^{-(\omega_{z1}+\omega_{z2})T_s} = 0 \\ &\Rightarrow z^2 - (r_1 + r_2)z + r_1 r_2 = 0 \\ &\text{where} \quad r_1 = e^{-\omega_{z1}T_s}; \quad r_2 = e^{-\omega_{z2}T_s}; \\ &\therefore z^2 + k_1 z + k_2 = 0 \end{aligned} \tag{29}$$

With

$$\begin{aligned} k_1 &= -(r_1 + r_2) \\ k_2 &= r_1 r_2 \end{aligned} \tag{30}$$

The discrete-time PID compensator and its discrete-time difference equation can now be expressed as:

$$G_{MAP}(z) = K_{cz}\frac{z^2 + k_1 z + k_2}{z(z-1)} = K_{cz}\frac{z^2 - (r_1 + r_2)z + r_1 r_2}{z(z-1)} \tag{31}$$

$$u[n] = u[n-1] + K_{cz}(e[n] - (r_1 + r_2)e[n-1] + r_1 r_2 e[n-2]) \tag{32}$$

For a crossover frequency f_x, the only unknown parameter K_{cz} of the digital PID is calculated from the following condition:

$$K_{cz} = \frac{z(z-1)}{z^2 - (r_1 + r_2)z + r_1 r_2}.G_c(s)|_{s=s_x} \tag{33}$$

As a result, the digital PID controller, numerically, is expressed by

$$G_{MAP}(z) = \frac{3.984z^2 - 7.391z + 3.427}{z^2 - z} \tag{34}$$

4.3. PID Controller with Derivative Filter

The continuous-time PID controller with a (first-order) derivative filter in parallel form is given by

$$\begin{aligned} G_c(s) &= \left[K_p + \frac{K_i}{s} + \frac{K_d s}{1+s/\omega_p}\right] = \left[K_p + \frac{K_i}{s} + \frac{K_d s}{1+T_f s}\right] \\ &= \frac{\left(K_p+K_d\omega_p\right)s^2+\left(K_p\omega_p+K_i\right)s+K_i\omega_p}{s\left(s+\omega_p\right)} \end{aligned} \tag{35}$$

where K_p, K_i, and K_d are controller parameters; T_f is a filter time constant. The low pass filter $1/(1 + T_f s)$ appended with derivative term $K_d s$ filters out the high-frequency noise entering the differentiator.

For computing the coefficients of the PID controller, a frequency response-based PID algorithm developed and patented by MathWorks [30] is used to achieve a good balance between performance (reference tracking and disturbance rejection, and so on) and robustness. The algorithm computes PID coefficients for a specific crossover frequency (loop bandwidth) based on the plant dynamics (usually one-tenth the switching frequency in case of switching converters), and a phase margin of 60°.

A brief theoretical description of the algorithm is outlined here. Once user-specified crossover frequency ω_x and phase margin θ_m are specified, the controller in the analog domain is expressed by [30]

$$G_c(s) = \frac{\omega_x}{s}\left(\frac{\sin\varphi_z s + \omega_x\cos\varphi_z}{\omega_x}\right)\left(\frac{\sin\beta s + \omega_x\cos\beta}{\sin\alpha s + \omega_x\cos\alpha}\right) \tag{36}$$

where the angles φ_z, α, and β lie in the range from 0° and 90°. The total phase shift $\Delta\phi$, a function of these angles, introduced by the PID at ω_x is given by

$$\Delta\phi = \varphi_z + \beta - \alpha \tag{37}$$

In the three-term product controller described in Equation (36), the first term refers to the integral action; the second term signifies the phase lead contributed by the K_p and K_i terms; the third term captures the phase lead introduced additionally by the K_d and T_f terms if $0° < \alpha < \beta < 90°$ and phase lag if $\beta < \alpha$. On the satisfaction of certain conditions or assumptions, the angles α and β that are the free parameters can be selected.

Running the MATLAB routine implementing the said algorithm, the PID controller in Equation (35) comes with the following coefficients:

$$K_p = 0.608,\ K_i = 1.41 \times 10^3,\ K_d = 5.82 \times 10^{-5},\ \text{and}\ T_f = 7.27 \times 10^{-6}.$$

Using these parameter values in Equation (35) and performing some algebraic manipulations, we obtain the following PID controller in a continuous domain.

$$G_c(s) = \frac{8.608s^2 + 8.494 \times 10^4 s + 1.941 \times 10^8}{s^2 + 1.375 \times 10^5 s} \tag{38}$$

The discrete-time PID controller obtained through the discretization of the continuous-time PID controller using Tustin transformation with T_s is then given by

$$G_{TUSTIN}(z) = \frac{4.35z^2 - 8.014z + 3.689}{z^2 - 0.9319z - 0.0682} \tag{39}$$

4.4. PID Controller with Derivative Filter—Direct Digital Design Approach

A discrete-time PID compensator with a filter can also be designed using a direct digital design (DDD) approach. In the DDD approach, a discrete-time compensator is directly constructed in the z-plane for a discretized plant. Like other cases, the considered DDD compensator is designed for $\Phi_m \geq 60$ and $\omega_x = \omega_x/10$.

Inspired by the work of [31], the DDD approach-based digital PIDF controller, in general form, is given by

$$G_{DDD}(z) = \frac{\widetilde{K}_i}{(z - w_d/\beta_d)} \times \frac{(z^2 - 2\zeta_d w_d z + {w_d}^2)}{(z-1)} \tag{40}$$

The two complex poles of the discretized forward converter (plant) are compensated by the two complex zeros of the digital compensator by placing them exactly at a position where the converter poles exist. In order to meet the requirement of steady-state error, a pole at $z = 1$ is placed. This gives $\widetilde{G}_{DDD}(z)$ as

$$\begin{aligned} \widetilde{G}_{DDD}(z) &= \left(\tfrac{z^2-1.97z+0.9773}{z-1}\right)\left(\tfrac{0.1149z+0.04927}{z^2-1.97z+0.9773}\right) \\ &= \tfrac{0.1149z+0.04927}{z-1} \end{aligned} \tag{41}$$

The gain M_g and the phase φ_g (to satisfy Φ_m) the controller needs to introduce at ω_x can be calculated from the complex value of $\widetilde{G}_{DDD}(z)$ at $z = e^{j\omega_x T_s}$ from $\widetilde{G}_{DDD}(e^{j\omega_x T_s}) = 0.2548e^{j1.4416}$, $M_g = 1/0.2548 = 3.9246$, and $\varphi_g = \Phi_m + 180 + 82.6$.

The remaining unknown parameters $\widetilde{K}_i$ and β_d of $G_{DDD}(z)$ can be determined by the following equations [31]:

$$\beta_d = \frac{\omega_d}{\frac{\sin(\omega_x T_s)}{\tan(\varphi_g)} + \cos(\omega_x T_s)} \tag{42}$$

$$\widetilde{K}_i = -M_g \sin(\omega_x T_s) \sin(\varphi_g) \left(1 + \frac{1}{\tan^2(\varphi_g)}\right) \tag{43}$$

Using ω_x, φ_g (in radians), and M_g in the above equations gives $\beta_d = 24.5349$ and $\widetilde{K}_i = 3.7979$. On knowing all the parameters, $G_{DDD}(z)$ takes the following form:

$$G_{DDD}(z) = \frac{3.798z^2 - 7.483z + 3.712}{z^2 - 1.04z + 0.04029} \tag{44}$$

This completes the digital controller design by the DDD approach.

The traditionally determined s-plane poles and zeros (or coefficients) of all the conventionally designed analog PID controllers are mapped approximately into z-plane poles and zeros (or coefficients) of digital PID controllers. Direct digital design approach-based controllers also require a discretized plant. This mapping from s-plane to z-plane thereby causes further distortions in frequency. The digital controllers only show limited performance, which can be enhanced by retuning the coefficients using the H–J pattern search method.

5. Digital Controller Optimization by the Hooke–Jeeves Method

Optimization of the discrete-time controllers is a multivariable unconstrained optimization problem, as no bounds are imposed on the PID controller coefficients. The Hooke–Jeeves (H–J) pattern search algorithm is employed to tune the coefficients (six in number) of conventionally designed digital controllers. The idea is to minimize the voltage error signal $e(t) = V_{out} - V_{ref}$ of the compensated forward converter system (in our case) as quickly as possible to ensure better reference tracking. This is accomplished by minimizing

the cost (error signal) in the form of the integral of the squared error (ISE). The cost function, in an n-multidimensional space, to be minimized thus takes the following form:

$$\text{ISE}: J = \int_0^\infty e^2(t)dt = \int_0^\infty \Big(V_{out}(t) - V_{ref}(t)\Big)^2 dt \tag{45}$$

The gradient-free H–J pattern search method [32], which uses a combination of exploratory moves and heuristic pattern moves iteratively, is proposed here to minimize J over $\Re^n$ without any constraints. The algorithm performs an exploratory move in the vicinity of the current point systematically to find the best point in the n-dimensional search space. Thereafter, n such points are used to make a pattern move. The steps involved in the H–J algorithm (in the form of Algorithm 1) are outlined below.

Algorithm 1. Hooke–Jeeves Pattern Search Algorithm.

Step 1: Set an initial guess (initial point or starting point) $x^{(0)} = (x_1^{(0)}, x_2^{(0)}, \ldots, x_n^{(0)}) \in \Re^n$, initial variable stepsizes $\Delta_i > 0$ $(i = 1, 2, \ldots, n)$, a step reduction parameter $\alpha > 1$, permissible error (termination parameter) $\varepsilon > 0$, and the maximum iterations $k_{\max}$. Set an iteration counter $k = 0$ and $x_p^{(k+1)} = x^{(0)}$.

Step 2: Execute an *exploratory move* with the base point $x^{(0)}$. Let the outcome of the exploratory move be x. If the exploratory move is a success, set $x^{(k+1)} = x$ and carry out Step 4; otherwise, carry out Step 3.

Step 3: Check the stopping (termination) criteria, i.e., if $\|\Delta_i\| < \varepsilon$ or $k \geq k_{\max}$, terminate; otherwise, set $\Delta_i = \Delta_i/\alpha$ for $i = 1, 2, \ldots, n$ and carry out Step 2.

Step 4: Set $k = k + 1$ and execute the *pattern move*: $x_p^{(k+1)} = x^{(k)} + (x^{(k)} - x^{(k-1)}) = 2x^{(k)} - x^{(k-1)}$.

Step 5: Execute another *exploratory move* using the base point $x_p^{(k+1)}$. Let the result be $x^{(k+1)}$.

Step 6: If $f(x^{(k+1)}) < f(x^{(k)})$, carry out Step 4; otherwise, carry out Step 3.

The algorithm takes the gains/coefficients (six in number for each case) of conventionally designed discrete-time controllers (initial guess) as the input. It comes with updated coefficients as the output, resulting in better performance and robustness. No constraint is imposed on the bounds of the design variables. The parameters of the H–J algorithm set for tuning all the controllers are summarized in Table 1.

Table 1. H–J pattern search method parameters.

H–J Method Parameters	Value
No. of variables N	6
Initial step sizes Δ	$(0.1, 0.1, 0.1, 0.1, 0.1, 0.1)^T$
Reduction factor α	2
Termination parameter ε	1×10^{-6}
Iteration counter k (initial value)	0
Fitness function (to be minimized) type	ISE
Maximum number of iterations	1000

The H–J algorithm, at the end of its execution, gives optimized discrete-time controllers with much improved transient response and steady-state error characteristics (see simulation results in the next section). Optimally-tuned and traditionally-tuned digital PID controller coefficients are detailed in Table 2. The number of iterations taken, and the objective function value attained finally by the optimized digital controllers are detailed in Table 3. It can be observed that the H–J method takes a different number of iterations to converge for different optimized digital controllers to achieve the same value of the objective function.

Table 2. Digital controller (traditional and optimized) coefficients.

No.	Digital Controller	Digital Controller Coefficients					
		a_2	a_1	a_0	b_2	b_1	b_0
1	$G_{MAP}(z)$	3.8620	−7.6100	3.7740	1	−1	0
	$G_{MAP\text{-}OPT}(z)$	3.8876	−7.6598	3.7991	0.5057	−0.3263	−0.1794
2	$G_{EULER}(z)$	4.205	−7.821	3.6360	1	−1	0
	$G_{EULER\text{-}OPT}(z)$	3.9413	−7.7655	3.8515	0.5129	−0.3312	−0.1816
	$G_{MAP}(z)$	3.9840	−7.3910	3.4270	1	−1	0
	$G_{MAP\text{-}OPT}(z)$	3.7290	−7.3473	3.6441	0.4855	−0.3135	−0.1720
3	$G_{TUSTIN}(z)$	4.3500	−8.0140	3.6890	1	−0.9319	−0.0682
	$G_{TUSTIN\text{-}OPT}(z)$	4.0156	−7.9121	3.9243	0.5225	−0.3372	−0.1854
4	$G_{DDD}(z)$	3.798	−7.483	3.712	1	−1.04	0.04029
	$G_{DDD\text{-}OPT}(z)$	3.8255	−7.5373	3.7383	0.4979	−0.3214	−0.1765

Table 3. The number of iterations taken, and the objective function value attained by the optimized controllers.

No.	Digital Controller	Resultant Objective Function Value	Iterations Taken for Convergence
1	$G_{MAP\text{-}OPT}(z)$	9.5637×10^{-6}	75
2	$G_{EULER\text{-}OPT}(z)$	9.5637×10^{-6}	102
	$G_{MAP\text{-}OPT}(z)$	9.5637×10^{-6}	71
3	$G_{TUSTIN\text{-}OPT}(z)$	9.5637×10^{-6}	92
4	$G_{DDD\text{-}OPT}(z)$	9.5637×10^{-6}	94

6. Simulation Results and Discussion

All the simulations were performed using the MATLAB/Simulink environment. The solver of type "fixed" was used to carry out all the simulations. As already mentioned, the forward converter system is designed to convert an input voltage V_{in} of 36 V to an output voltage V_{out} of 12 V. The H–J pattern search algorithm is used to optimize digital controllers. The performance of digital controllers, unoptimized and optimized, for a fixed load (10 Ω) is presented in Figure 6, for all three cases. Inspection of output voltage response reveals that the optimized digital controllers offered better transient response characteristics than their unoptimized counterparts. A detailed comparison of transient response characteristics extracted from voltage responses is given in Table 4.

Table 4. The performance offered by digital PID controllers.

No.	Digital Controller	Transient Response Characteristics				
		Rise Time t_r (s)	Settling Time t_s (s)	Overshoot M_r (%)	Peak Value h_{peak} -	Peak Time t_{peak} (s)
1	$G_{MAP}(z)$	3.1607×10^{-5}	8.1243×10^{-5}	4.4132	12.5296	6.6667×10^{-5}
	$G_{MAP\text{-}OPT}(z)$	1.6429×10^{-5}	4.1968×10^{-5}	5.1647	12.6198	3.3333×10^{-5}
2	$G_{EULER}(z)$	2.6836×10^{-5}	7.5744×10^{-5}	21.5128	14.5815	6.6667×10^{-5}
	$G_{EULER\text{-}OPT}(z)$	1.6459×10^{-5}	4.1984×10^{-5}	5.1910	12.6229	3.3333×10^{-5}
	$G_{MAP}(z)$	2.7852×10^{-5}	7.4965×10^{-5}	21.9312	14.6317	6.6667×10^{-5}
	$G_{MAP\text{-}OPT}(z)$	1.6496×10^{-5}	4.1988×10^{-5}	5.1748	12.6210	3.3333×10^{-5}
3	$G_{TUSTIN}(z)$	2.6829×10^{-5}	6.7370×10^{-5}	21.3563	14.5628	6.6667×10^{-5}
	$G_{TUSTIN\text{-}OPT}(z)$	1.6452×10^{-5}	4.1979×10^{-5}	5.1564	12.6188	3.3333×10^{-5}
4	$G_{DDD}(z)$	3.0780×10^{-5}	8.6204×10^{-5}	6.1813	12.7418	6.6667×10^{-5}
	$G_{DDD\text{-}OPT}(z)$	1.6472×10^{-5}	4.1983×10^{-5}	5.1679	12.6202	3.3333×10^{-5}

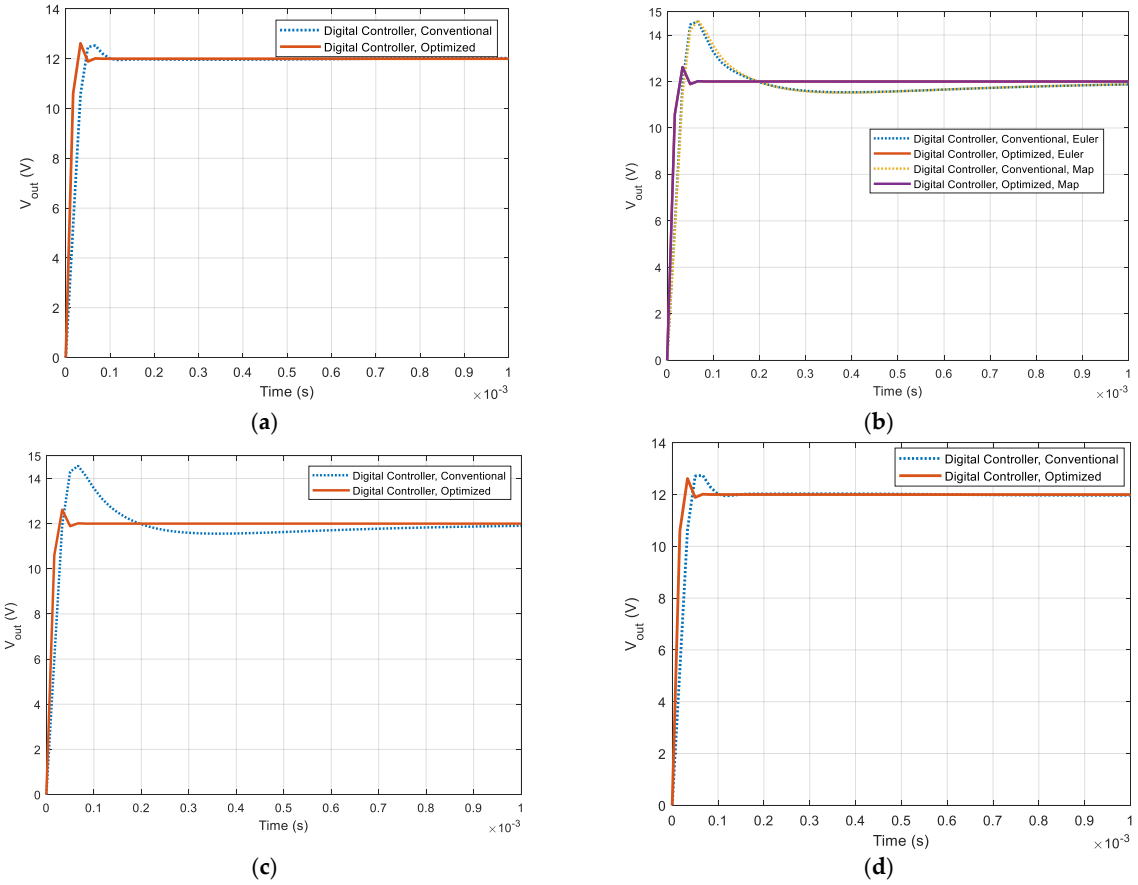


Figure 6. Voltage response offered by digital controllers of (**a**) case 1, (**b**) case 2, (**c**) case 3, and (**d**) case 4.

To compare the results of the deterministic H–J method with other stochastic optimization methods, a simulated annealing (SA) algorithm that mimics the thermodynamic process of metal annealing was considered. Both H–J and SA are gradient-free algorithms and solve unconstrained optimization problems well. Both the algorithms take the traditionally-tuned discrete PID controllers' coefficients as the initial point or guess.

For simulation purposes, the most commonly used (standard) values of SA parameters were considered, which are summarized in Table 5.

Table 5. Simulated annealing (SA) parameters taken for simulations.

SA Parameter	Value
Cost function f	ISE
Initial temperature T_0	100
Annealing function	Fast annealing
Initial acceptance probability	1
Acceptance probability function p	$p(\Delta, T) = \left[1 + \exp\left(\frac{\Delta}{\max(T)}\right)\right]^{-1} \in [0, 0.5]$ where $\Delta = f_{new} - f_{old}$
Temperature update function T	$T = T_0 \times 0.95^k$ where k signifies the annealing parameter.
Reannealing interval	100
Function tolerance (termination criteria)	1×10^{-6}
Maximum function evaluations	18,000

Considering case 2, the output voltage response offered by SA showed somewhat increased overshoot and steady-state error than that of the H–J method (see Figure 7). This justifies the applicability of the H–J method to digital controllers. It can be further deduced that an unconstrained optimization problem involving fewer decision variables can be handled well by a deterministic optimization algorithm compared to a stochastic optimization algorithm.

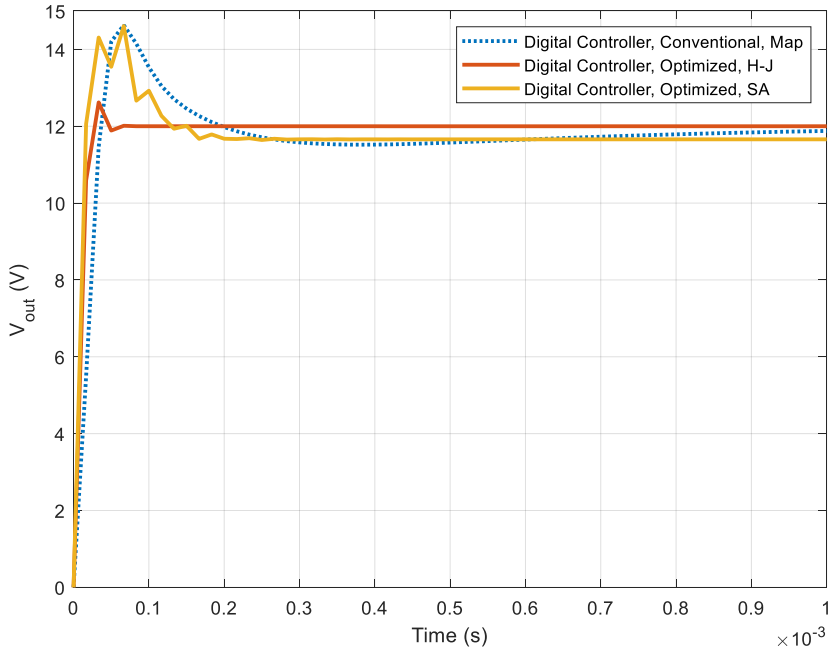


Figure 7. Voltage response offered by optimized digital controllers.

All additional simulations were carried out using the digital PID controllers, unoptimized and optimized (by the H–J method), of case 3 to save space. The error signal became minimized more quickly in the case of the optimized compensated system (see Figure 8). This ensured better reference tracking and transient response characteristics. To gain insight into the H–J optimization method further, the cost function representing the integral of the squared error (ISE) was plotted against the iteration, as shown in Figure 9. As can be observed, with the progression of iteration, the cost function decreased monotonically and finally converged to a value of 9.5637×10^{-6} after meeting the stopping criteria. The algorithm took 513.252875 s for 92 iterations when run on a personal computer with a Core i7 (2.10 GHz) processor and 8 GB of RAM. This minimization of cost function resulted in better convergence of the output (voltage) to the set point. Figure 10 shows that optimized digital controllers follow the changes in reference voltage from 12 V to 18 V and 18 V to 12 V more quickly compared to their unoptimized counterparts. This justifies the claim of superiority of the performance of optimized controllers over unoptimized ones.

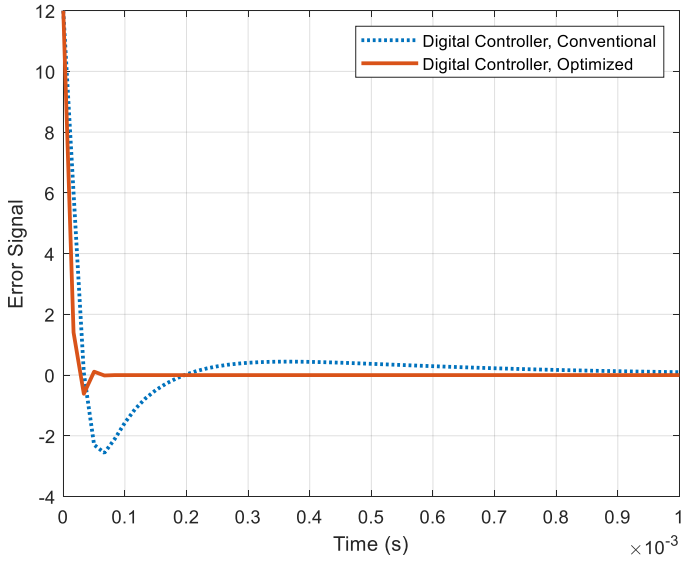


Figure 8. The error signal generated in unoptimized and optimized compensated systems.

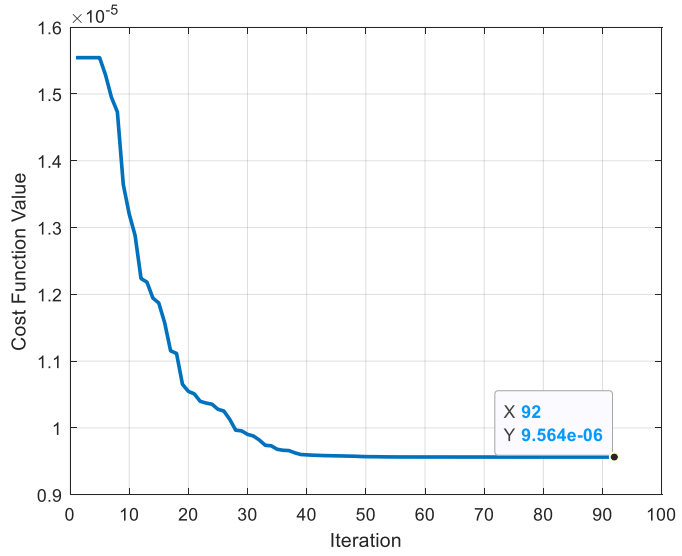


Figure 9. Variation of the cost function with iteration.

For the real compensated forward converter system, nonlinear effects due to ADC and DAC, and delay in the digital control loop should be taken into consideration as they impose adverse effects on performance [33]. For the design example, ripples in output voltage ΔV were considered 1% of V_{out} and V_{ref} 80% of V_{max}. The detail of the digital control loop nonlinearities with numeric values is summarized in Table 6.

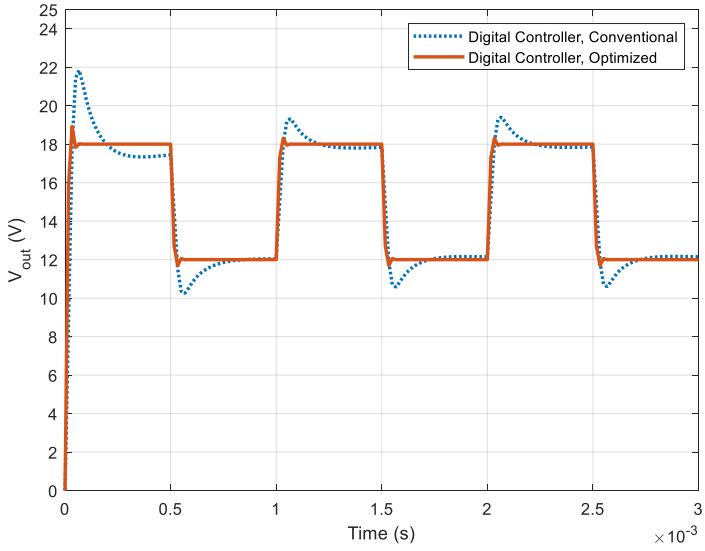


Figure 10. Reference tracking by digital controllers.

Table 6. Detail of the digital control loop nonlinearities.

Term	Formula	Value
ADC resolution n_{ADC}	$n_{ADC} \geq \text{int}\left[\log_2\left(\frac{V_{\max}}{V_{ref}} \cdot \frac{V_{out}}{\Delta V_{out}}\right)\right]$	7
DAC resolution n_{DAC}	$n_{DAC} \geq \text{int}\left[n_{ADC} + \log_2\left(\frac{V_{ref}}{V_{\max} \cdot D}\right)\right] \simeq n_{ADC} + 1$	8
ADC gain K_{ADC}	$K_{ADC} = 2^{n_{ADC}}$	128
DAC gain K_{DAC}	$K_{DAC} = 1/(2^{n_{DAC}} - 1)$	0.0039
Loop delay t_d	$t_d = \underbrace{t_{ADC} + t_{DAC}}_{\text{ADC/DAC Conversion}} + \underbrace{t_P}_{\text{Processing}} + \underbrace{t_{GD}}_{\text{Gate Driver}}$	$0.5T_s$
Delay transfer function $G_d(s)$	$G_d(s) = e^{-st_d} \simeq 1/(1 + st_d)$	-

Using the PID algorithm developed by MathWorks (Case 3), the digital controller transformed through Tustin for the modified plant $T_p(s)\big|_{\text{modf}} = e^{-st_d} K_{ADC} K_{DAC} T_p(s)$ now is computed to be

$$G_{TUSTIN}(z) = \frac{15.87z^2 - 29.68z + 13.87}{z^2 - 0.0542z - 0.9458} \tag{46}$$

Furthermore, optimization of the above newly-designed digital PID controller through the H–J method gives optimized digital PID controller as

$$G_{TUSTIN-OPT}(z) = \frac{20.1581z^2 - 34.4638z + 14.3793}{z^2 - 0.4230z - 0.5763} \tag{47}$$

To justify that the optimized PID controller offers excellent load regulation compared to the unoptimized one, a change in load resistance was made from 10 Ω to 5 Ω and 5 Ω to 10 Ω. From the transient load response shown in Figure 11, it is clear that the optimized PID controller offered a reduced voltage spike and recovery time at the instant of load transient compared to the unoptimized compensator. Similarly, despite the changes in the input voltage from 36 V (nominal) to 48 V and then from 48 V to 36 V, the controllers maintained a constant output voltage of 12 V (see Figure 12). However, in the instant of a change in the input voltage, the optimized controller showed less deviation in the output voltage value and settled the output voltage to its steady-state value more quickly compared to its

unoptimized counterpart. The optimized controller, thus, exhibited excellent load and line regulation.

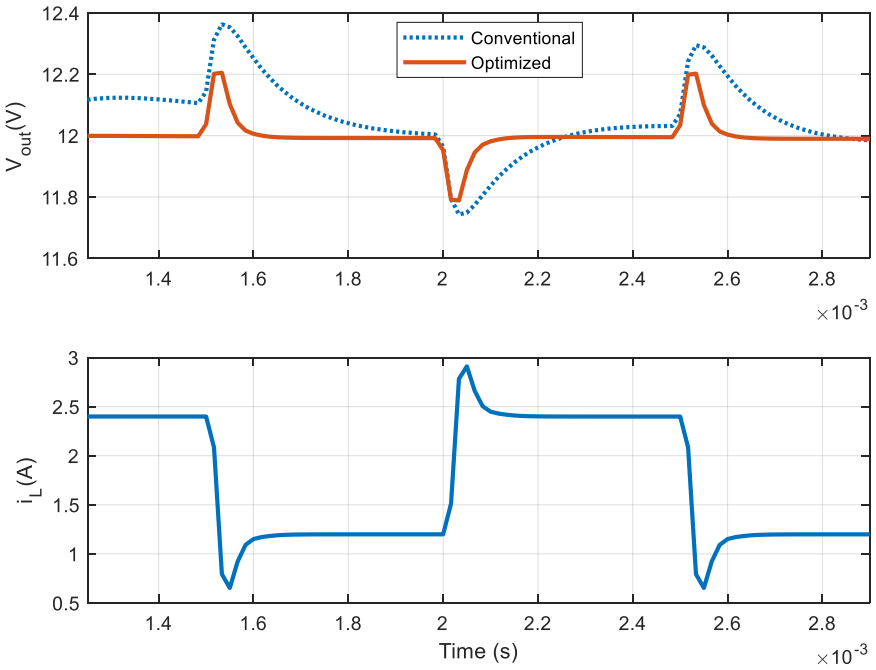


Figure 11. Load transient response offered by digital PID controllers.

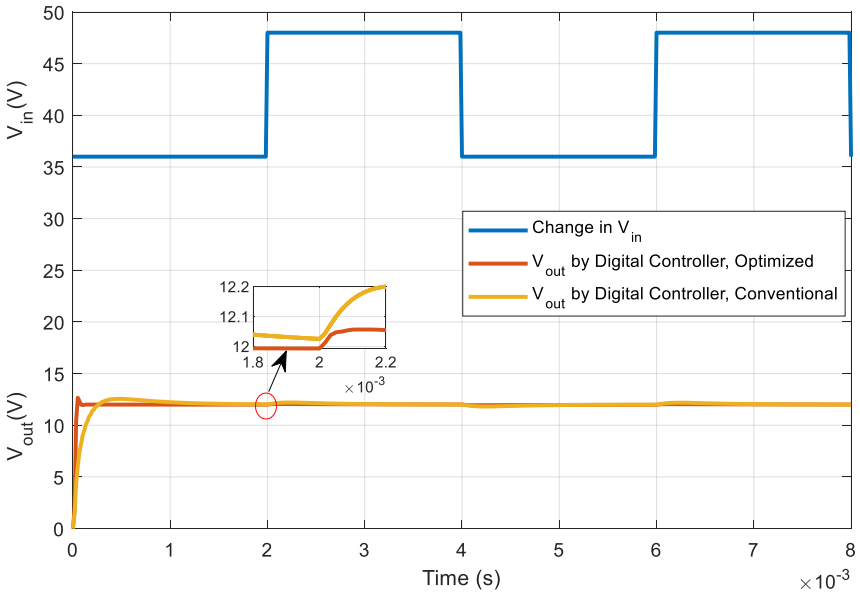


Figure 12. Line regulation offered by digital PID controllers.

The tuning of all considered digital PID controllers with and without nonlinearities by the H–J search method always resulted in better control performance. This justifies the applicability and workability of the once scorned but now respectable H–J pattern search method.

7. Hardware-into-the-Loop Implementation

For the sake of rapid prototyping, a Xilinx System Generator (XSG), a DSP design tool from Xilinx [34], is used for implementing the discrete-time PID controller on FPGA that

can be easily interfaced with Simulink through the XSG environment. Once integrated with Simulink, XSG automatically produces low-level, executable, synthesizable, and vendor-neutral VHDL code (for the control algorithm) from the Simulink model-based generated high-level abstractions. This way, sophisticated and complex digital control algorithms are realized rapidly on FPGA compared to conventional resistor–transistor logic (RTL) development times by control design engineers without having expertise in developing VHDL code. This reduces design and testing time.

The netlist and cores are generated automatically through the Core Generator and ChipScope generator invoked by XSG. Consequently, the generated bitstream—the co-simulation FPGA configuration file for the JTAG hardware co-simulation platform—is loaded into the target device (FPGA XC7A35T-1CPG236C on Basys 3 Artix-7 FPGA board, in our case), thus implementing the digital controller on FPGA.

The optimized controller in Equation (47) is considered for the hardware into the loop (HiL) implementation and is re-written as

$$G_{TUSTIN-OPT}(z) = \frac{U(z)}{E(z)} = \frac{20.1581 - 34.4638z^{-1} + 14.3793z^{-2}}{1 - 0.4230z^{-1} - 0.5763z^{-2}} \tag{48}$$

Furthermore, in the difference equation form, the above controller takes the form

$$\begin{aligned} u(k) \quad &= 20.1581e(k) - 34.4638e(k-1) + 14.3793e(k-2) + 0.4230u(k-1) \\ &+0.5763u(k-2) \end{aligned} \tag{49}$$

For realizing the above digital controller, hardware-realizable adders/subtractors, multipliers, and delay blocks from the XSG library are used (see Figure 13). The 32-bit floating-point arithmetic (FP) is employed to realize the controller coefficients. The relatively fast FP arithmetic ensures certain accuracy for realizing coefficients. Rather than using direct programming (DP), standard programming (SP) is employed here to realize the controller. SP uses only n delay elements, whereas DP uses $m + n$, where m and n denote the number of zeros and poles, respectively, such that $m \leq n$ [35].

A synthesizable VHDL block representing the hardware co-simulation library is then generated automatically and is loaded into the Artix-7 board (see Figure 13). For downloading the bitstream, JTAG communication between Simulink (on PC) and hardware platform (Artix-7 FPGA board) for a supported board is performed. This way, hardware–software co-simulation through JTAG is accomplished to close the digital control loop.

After introducing hardware into the control loop, it has been observed that the XSG-based compensated system displays almost the same output voltage response as that of the Simulink-based compensated system, as shown in Figure 14, thus validating the HiL implementation. This is quite understandable, as the floating-point data format for digital controller coefficients has been used just like the "double" type data of Simulink.

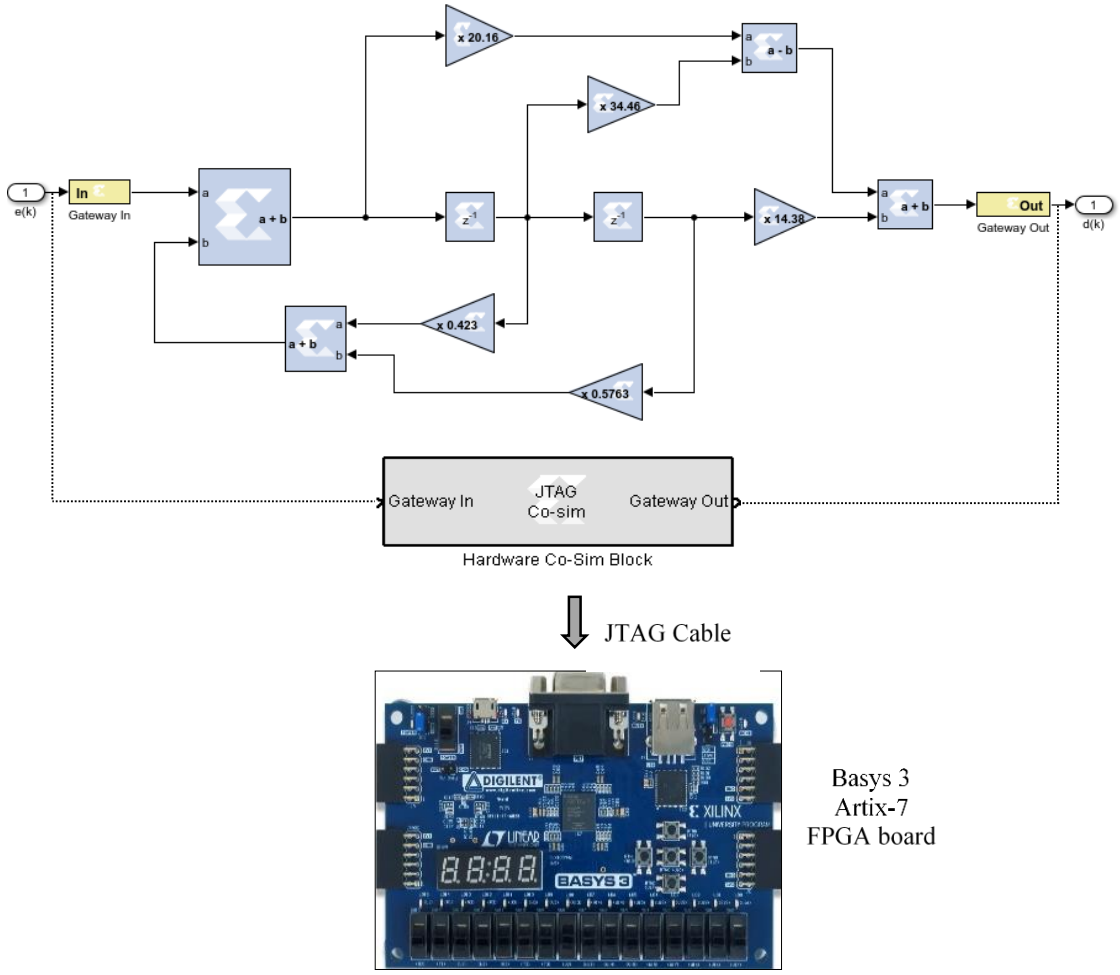


Figure 13. Hardware–software co-simulation framework for realizing the digital PID controller.

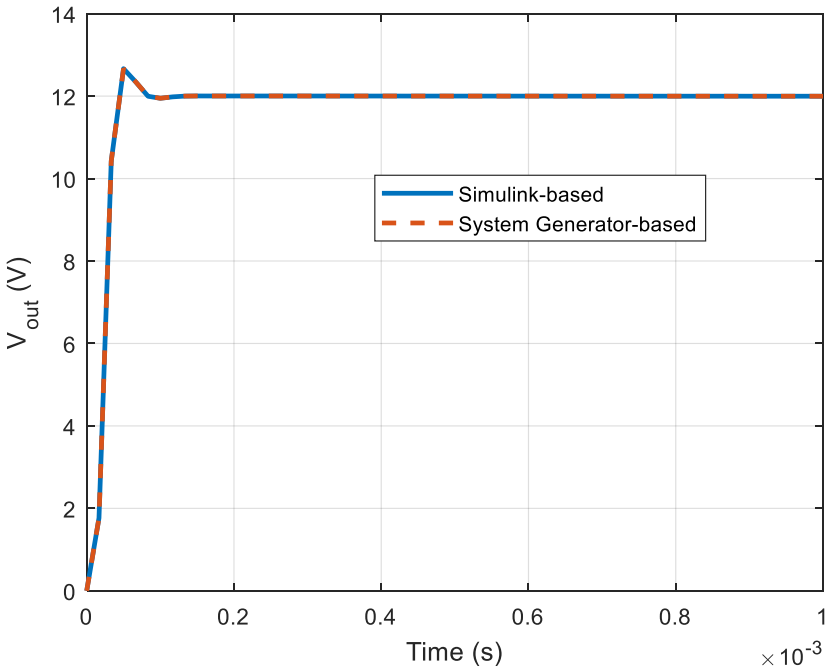


Figure 14. Output voltage response by Simulink and System Generator.

8. Conclusions

In this paper, the Hooke Jeeves search algorithm was successfully applied to tune the coefficients of discrete-time PID controllers to enhance the performance of the compensated forward DC–DC converter. Three types of PID controllers were designed on the basis of frequency response characteristics (crossover frequency and phase margin) in the *s*-plane, which were then mapped into the *z*-plane using transformation techniques such as Tustin, backward Euler, and (simple) mapping. The digital redesign approach based designed digital PID controllers show only nominal performance, which further gets deteriorated due to frequency distortions during mapping and nonlinearities such as ADC and DAC, sampling and hold effects, loop delay, and so on. Based on our findings, we observe that when the H–J pattern search method is applied to these conventionally-designed digital controllers (with and without nonlinear elements) exhibiting limited performance, it fine-tunes the controller coefficients intelligently by minimizing the cost function rapidly, thus ensuring the near-optimal solution. For all the considered cases, better control performance is achieved. This clearly indicates that the H–J method employs pattern search efficiently to make the iterative process fast-convergent. Hardware-into-the-loop implementation is also carried out for rapid prototyping.

Author Contributions: Conceptualization, G.A.; methodology, G.A., M.U.A., V.E.B., M.R.H., and J.G.; software, U.F. and S.A.; validation, C.C. and A.R.; formal analysis, G.A., A.B.A., and U.F.; investigation, G.A. and U.F.; resources, V.E.B. and M.R.H.; data curation, A.R., M.U.A., and A.B.A.; writing—original draft preparation, G.A. and M.U.A.; writing—review and editing, U.F. and M.U.A.; visualization, S.A., J.G., and C.C.; supervision, J.G.; project administration, G.A. and M.U.A.; funding acquisition, V.E.B., M.R.H., and S.A. All authors have read and agreed to the published version of the manuscript.

Funding: This research is financially supported by the Deanship of Scientific Research at King Khalid University under research grant number (R.G.P2/100/41).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Acknowledgments: The authors would like to express their gratitude to The University of Lahore for administrative and technical support.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Jin, X.; Wan, L.; Xu, J.; Qian, B.; Lu, Z. Dual-switch forward converter with an additional reset capacitor for hold-up operation. *J. Eng.* **2019**, *2019*, 2593–2596. [CrossRef]
2. Klassen, S.V.; Klassen, T.S.; Shtein, D.A.; Volkov, A.G.; Dubkova, R.Y.; Luft, S.V. Study of a Dual-Loop Subordinate Control System for a DC-DC Converter with Galvanic Isolation. In Proceedings of the 2018 19th International Conference of Young Specialists on Micro/Nanotechnologies and Electron Devices (EDM), Erlagol, Russia, 29 June–3 July 2018; pp. 6403–6410.
3. Qu, L.; Zhang, D.; Bao, Z. Output Current-Differential Control Scheme for Input-Series–Output-Parallel-Connected Modular DC–DC Converters. *IEEE Trans. Power Electron.* **2016**, *32*, 5699–5711. [CrossRef]
4. Sha, D.; Guo, Z.; Liao, X. Digital Control Strategy for Input-Series-Output-Parallel Modular DC/DC Converters. *J. Power Electron.* **2010**, *10*, 245–250. [CrossRef]
5. Mahmood, K.S.; Hasan, I.; Iqbal, M.M. Modeling and Closed Loop Voltage Mode Control of a Forward Converter. *Indian J. Sci. Technol.* **2019**, *12*, 1–15. [CrossRef]
6. Singh, S.; Singh, B.; Bhuvaneswari, G. MOHF Forward Buck DC-DC Converter Based SMPS. *Asian Power Electron. J.* **2012**, *6*, 28–33.
7. Xu, C.; Ma, Q.; Xu, P.; Wang, N. Closed-Loop Gate Drive for Single-Ended Forward Converter to Reduce Conducted EMI. *IEEE Access* **2020**, *8*, 123746–123755. [CrossRef]
8. Cheng, K.-H.; Hsu, C.-F.; Lin, C.-M.; Lee, T.-T.; Li, C. Fuzzy–Neural Sliding-Mode Control for DC–DC Converters Using Asymmetric Gaussian Membership Functions. *IEEE Trans. Ind. Electron.* **2007**, *54*, 1528–1536. [CrossRef]
9. Li, Z.-Q.; Zhang, X.-L.; Wen, X. Simulation Research on Control Strategy for Push-pull Forward DC-DC Converter. In Proceedings of the 2016 International Conference on Computer Engineering and Information Systems, Shanghai, China, 12–13 November 2016; Atlantis Press: Paris, France, 2016.

10. Hsu, C.-F.; Chung, I.-F.; Lin, C.-M.; Hsu, C.-Y. Self-regulating fuzzy control for forward DC–DC converters using an 8-bit microcontroller. *IET Power Electron.* **2009**, *2*, 1–13. [CrossRef]
11. Alex, L.T.; Dash, S.S.; Sridhar, R. Performance Analysis of Modular Forward Converter in Input Parallel Output Series (IPOS) Architecture Using PI and Fuzzy Logic Controller. *Int. J. Fuzzy Syst.* **2019**, *21*, 1524–1532. [CrossRef]
12. Janga, R.; Malaji, S. Performance evaluation of active clamp forward converter with fuzzy logic controller. In Proceedings of the 2017 International Conference on Intelligent Computing and Control (I2C2), Coimbatore, India, 23–24 June 2017; pp. 1–6.
13. Talbi, S.; Mabwe, A.M.; El Hajjaji, A. PI-fuzzy control of a bidirectional Dual Active Bridge converter. In Proceedings of the 2017 American Control Conference (ACC), Seattle, WA, USA, 24–26 May 2017; pp. 1271–1277.
14. Baby, A.; Nithya, M. Sliding mode controlled forward converter. In Proceedings of the 2015 IEEE 9th International Conference on Intelligent Systems and Control (ISCO), Coimbatore, India, 9–10 January 2015; pp. 1–4.
15. Wang, G.; Chadli, M.; Basin, M. Practical terminal sliding mode control of nonlinear uncertain active suspension systems with adaptive disturbance observer. *IEEE/ASME Trans. Mechatron.* **2020**. [CrossRef]
16. Nguyen, N.P.; Mung, N.X.; Thanh Ha, H.L.N.; Huynh, T.T.; Hong, S.K. Finite-Time Attitude Fault Tolerant Control of Quadcopter System via Neural Networks. *Mathematics* **2020**, *8*, 1541. [CrossRef]
17. Kobaku, T.; Jeyasenthil, R.; Sahoo, S.; Ramchand, R.; Dragicevic, T. Quantitative Feedback Design Based Robust PID Control of Voltage Mode Controlled DC-DC Boost Converter. *IEEE Trans. Circuits Syst. II Express Briefs* **2020**. [CrossRef]
18. Xu, S.; Ye, Z. Digital voltage feed-forward control for isolated DC/DC converters. In Proceedings of the 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 17–21 May 2013; pp. 2112–2117.
19. Hwu, K.I. Forward Converter with FPGA-Based Self-Tuning PID Controller. *Tamkang J. Sci. Eng.* **2010**, *13*, 173–180.
20. Baek, J.; Youn, H.-S. Full-Bridge Active-Clamp Forward-Flyback Converter with an Integrated Transformer for High-Performance and Low Cost Low-Voltage DC Converter of Vehicle Applications. *Energies* **2020**, *13*, 863. [CrossRef]
21. Dimitrov, B. Direct Off-Line Two-Switch Forward Converter with a Boost PFC Converter for Powering of DC Electromagnet Systems. *TEM J.* **2018**, *7*, 3–12.
22. Abbas, G.; Farooq, U.; Gu, J.; Asad, M.U. Constrained Model-Based Predictive Controller for a High-Frequency Low-Power DC-DC Buck Converter. *Int. J. Electr. Eng. Inform.* **2013**, *5*, 316–339. [CrossRef]
23. Middlebrook, R.D.; Cuk, S. A general unified approach to modelling switching-converter power stages. In Proceedings of the 1976 IEEE Power Electronics Specialists Conference, Cleveland, OH, USA, 8–10 June 1976; pp. 18–34.
24. Abbas, G.; Farooq, U.; Gu, J.; Asad, M.U. An improved PID controller for switching converters. In Proceedings of the Proceeding of the 11th World Congress on Intelligent Control and Automation, Shenyang, China, 29 June–4 July 2014; pp. 1445–1450.
25. Rymarski, Z.; Bernacki, K. Different Features of Control Systems for Single-Phase Voltage Source Inverters. *Energies* **2020**, *13*, 4100. [CrossRef]
26. Abbas, G.; Farooq, U.; Asad, M.U. Design and FPGA implementation of 1-degree-of-freedom discrete PID controller for power switching converter. In Proceedings of the 2012 7th IEEE Conference on Industrial Electronics and Applications (ICIEA), Singapore, 18–20 July 2012; pp. 1070–1074.
27. Ounis, F.; Golea, N. PID, 2-DOF PID and Mixed Sensitivity Loop-Shaping Based Robust Voltage Control of Quadratic Buck DC-DC Converter. *Adv. Electr. Electron. Eng.* **2016**, *14*, 551–561. [CrossRef]
28. Wang, B.; Zhang, X.; Ye, J.; Gooi, H.B. Deadbeat Control for a Single-Inductor Multiple-Input Multiple-Output DC–DC Converter. *IEEE Trans. Power Electron.* **2018**, *34*, 1914–1924. [CrossRef]
29. Prodic, A.; Maksimović, D.; Erickson, R.W. Design and implementation of a digital PWM controller for a high-frequency switching DC-DC power converter. In Proceedings of the IECON'01—27th Annual Conference of the IEEE Industrial Electronics Society (Cat. No. 37243), Denver, CO, USA, 29 November–2 December 2001; Volume 2, pp. 893–898.
30. Gahinet, P.; Chen, R.; Eryilmaz, B. Automated PID Controller Design. U.S. Patents 12/604,924, 18 June 2013.
31. Cuoghi, S.; Ntogramatzidis, L.; Padula, F.; Grandi, G. Direct Digital Design of PIDF Controllers with ComPlex Zeros for DC-DC Buck Converters. *Energies* **2019**, *12*, 36. [CrossRef]
32. Hooke, R.; Jeeves, T.A. Direct Search Solution of Numerical and Statistical Problems. *J. ACM* **1961**, *8*, 212–229. [CrossRef]
33. Abbas, G.; Gu, J.; Farooq, U.; Abid, M.I.; Raza, A.; Asad, M.U.; Balas, V.E.; Balas, M.E. Optimized Digital Controllers for Switching-Mode DC-DC Step-Down Converter. *Electronics* **2018**, *7*, 412. [CrossRef]
34. System Generator for DSP. Available online: https://www.xilinx.com/products/design-tools/vivado/integration/sysgen.html (accessed on 18 August 2020).
35. Abbas, G.; Nazeer, M.Q.; Balas, V.E.; Lin, T.-C.; Balas, M.M.; Asad, M.U.; Raza, A.; Shehzad, M.N.; Farooq, U.; Gu, J.; et al. Derivative-Free Direct Search Optimization Method for Enhancing Performance of Analytical Design Approach-Based Digital Controller for Switching Regulator. *Energies* **2019**, *12*, 2183. [CrossRef]