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FPGA BASED STANDALONE EMBEDDED WEB SERVER FOR REMOTE CONTROL OF DISPLAY DEVICES

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Abstract

The Field Programmable Gate Array (FPGA) devices are quickly replacing the microcontrollers for embedded applications since they offer both the performance of hardware and flexibility of software computing. Custom logic design implementation can be done using FPGAs for faster control systems and it also adds the advantage of parallel processing which are not available in processors and controllers that works sequentially for embedded systems. Integrating web server functionality with these devices offers remote access and controls them over Internet in the form of web pages on a web browser. This work presents the concept of creating an embedded web server using APSOC and FPGA to control a Video Graphics Array (VGA) display remotely through Internet. The proposed system has been designed and first implemented in Nexys 3, development platform based on Xilinx Spartan-6 LX 16 FPGA, then finally on ZYNQ-7000 APSOC (Zybo).

Keywords:

FPGA, Embedded Web Server, Internet

1. INTRODUCTION

The Field Programmable Gate Array (FPGA) devices are quickly replacing the microcontrollers and mask programmable devices for embedded applications since they offer both hardware and software flexibility of computing. Custom logic design implementation can be done using FPGAs for faster control systems and it also adds the advantage of parallel processing which are not available in processors and controllers that works sequentially for embedded systems. Integrating webserver functionality with these devices offers remote access and control. This work presents the concept of creating an embedded web server using FPGA to control Video Graphics Array (VGA) display remotely through internet. Here hardware is processing the data and there exist no software overheads. In contrast with the processor based system which executes sequentially rather FPGA receives and processes the data from the server, thereby thrown parallel for the display. This makes the overall process faster. Since, only a part of the hardware is active it consumes less power. Another added advantage is that the hardware is reconfigurable. Even if display unit is changed or the network has opted for a different speed the hardware inside FPGA can be reprogrammed. Chavan et al. [6] discussed about the design of embedded web server based on Ethernet technology for remote monitoring of weather parameters.

This web server monitors parameters viz. temperature and humidity and transmits this information in the form of HTML web-page. They used LM35 semiconductor temperature sensor and SY-HS-220 humidity module. Deepak et al. [9] designed a EWS for monitoring and controlling home appliances via web browser. At the same time, users can monitor the security situation at home in real-time through different sensors installed at the home. They used low cost WIZ220IO as the embedded web server for implementation of the prototype remotely via internet. Aby Thomas [13] proposed a model for monitoring temperature and CO2 in industry using embedded web server. The system consists of an ARM cortex processor LPC1768 with an integrated Ethernet interface and the whole system can function as a web server. They used this system to monitor the temperature and concentration of CO2 in the industry. For monitoring temperature and gas concentration they used LM35 temperature sensor and CO2 gas sensor. The web page shows three data. The first data is the temperature, second data is concentration of CO2 gas and third data shows that the motor for fan control is on when the temperature has risen above a cut of value the fan becomes on to cool the remote industrial area. Srinivas Raja et al. [21] proposed Remote monitoring system based on chip microprocessor. The chip microprocessor transplanted TCP/IP protocol is configured to an embedded web server which has data collection, storage and communication functions. In various Internet applications based on client server architecture, it is better to use embedded WEB server other than PC server for decreasing volume, cost and power consumption. Fang Hongping et al. [22] presented Remote monitoring system based on embedded web server through which connects any electronic device to web server and can get the real time data of devices through the web pages released by the server. The method can overcome the problem of PC based monitoring system. Young-tao Zhou et al. [23] designed a proxy server for PC in which TCP/IP protocols are realized so that it can be connected to the Internet. Pawan Kumar et al. [28] implemented a GSM based electronic notice board using 8051 micro controller. The controller receives the message through the GSM MODEM and displays it in LCD.

2. PREVIOUS WORKS

2.1 GSM BASED E-NOTICE BOARD

The SMS driven automatic display toolkit is used to replace programmable electronic display. This toolkit can be programmed from an authorized mobile phone. The message to be displayed is sent through a SMS from an authorized transmitter. The toolkit receives the SMS, validates the sending Mobile Identification Number (MIN) and displays the desired information after necessary code conversion. The system is made efficient by using 'clone' SIMs of same MIN in a geographical area so that the same SMS can be received by number of display boards in a locality using techniques of time division multiple access. The display board programs itself with the help of the incoming SMS with proper validation. Such a system proves to be helpful for immediate information transfer. The system required for the purpose is nothing but a Microcontroller based SMS box. The main components of the toolkit include microcontroller and a

GSM modem. These components are integrated with the display board and thus incorporate the wireless features. The GSM modem receives the SMS. The AT commands are serially transferred to the modem through MAX232. In return the modem transmits the stored message through the COM port. The microcontroller validates the SMS and then displays the message in the LCD display board. Various time division multiplexing techniques have been suggested to make the display boards functionally efficient.

2.2 EMBEDDED WEB SERVER-BASED HOME APPLIANCE NETWORKS

The Internet has been mostly used to connect personal computers so far, but shortly all kinds of appliances with embedded computers will exchange information over the Internet. A massive number of microcontrollers are available in today's devices when these intelligent devices are connected to the Internet, the way the user control and manage their functions would change entirely. Web pages are be used as user interfaces where each appliance has the ability to serve its user interface as a web page over the Internet. These pages can contain not only text but also pictures, hypertexts, photographs, video and audio as in usual web pages. By the advent of the user interfaces based on web pages, all devices requiring user interaction can be controlled and managed from one device which includes a web browser, such as a personal digital assistant, cell phone, etc. Also, use of web page based, button and display free designs reduce the cost of production while making the systems more user-friendly. Remote control via the Internet is not a new feature and used in home automation systems. However, providing a mechanism for interaction between devices in this environment is quite challenging. For example, an alarm clock can interact with the heating system according to the alarm time and can send instructions to the heating system to start warming the house before the residents wake up. There exist some commercial platforms, which facilitate the development of applications interacting with and exploiting the abilities of networked intelligent devices. This system is not similar to these platforms. However, all solutions including aims at the same features, namely supporting remote control of devices via the Internet and providing a mechanism for interaction between devices.

2.3 EMBEDDED WEB SERVER MONITORING SYSTEM AND CDMA SERVICE

Remote monitoring systems based on web-server-embedded technology and mobile telecommunication will become a core node technology in sensing network construction because of a great deal of mobile users and spreads of digital services in next generation telecommunication in the world. Soil, environmental, and crop information monitoring are important in production management and decision making in precision agriculture. Therefore, reliability, security and inexpensive characteristics required will be essential in the crop field information monitoring. Three improved field monitoring servers (FMS) using code division multiple access (CDMA) services combined with IP Sec-based virtual private network (VPN) function have installed to two rice practical fields in Shanghai and one maize experimental field in Beijing for constructing a remote wireless sensing network. This crop field remote monitoring system as a ubiquitous node infrastructure in wireless sensing networks is useful and powerful to collect soil, environment, and crop information in remote for precision agriculture. The real-time soil and environment data, and crop images can be dynamically collected in remote area by the crop field monitoring systems.

3. PROPOSED SYSTEM

The embedded web server is created using Nexys 3, spartan 6 FPGA development board.

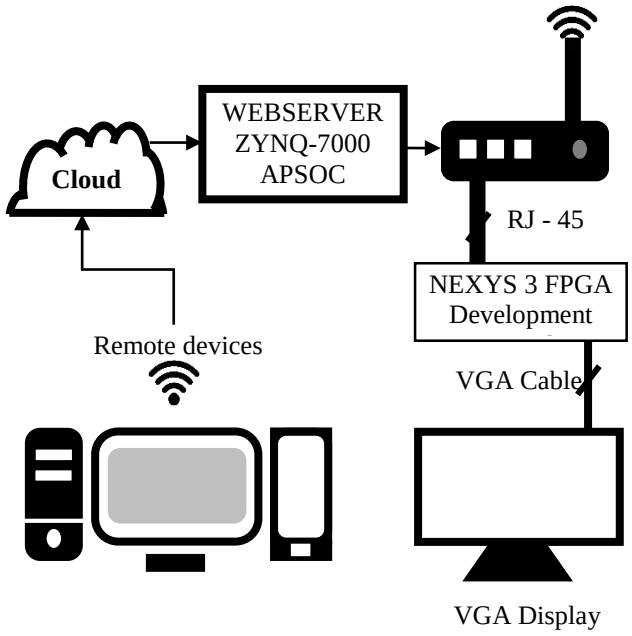

Fig.1. Block diagram of proposed system

The Ethernet port is configured with the IP address 192.168.0.44 and 1024 as port ID. User datagram protocol (UDP) is chosen with 18 byte as data payload. The block diagram of the proposed system is shown in Fig.1. The remote devices can access the Nexys 3 board via Internet which is connected with the router through RJ-45 cable. The received data is bypassed to UART for debugging purpose. The received data is matched with the character set for displaying the corresponding character in the VGA display.

4. SOFTWARE/HARDWARE SPECIFICATION

4.1 SOFTWARE SPECIFICATION

Xilinx ISE Simulator is a Hardware Description Language (HDL) simulator that enables to perform functional and timing simulations for VHDL, Verilog and mixed-language designs. The Xilinx ISE Design Suite provides an integrated flow with the ISE Simulator that allows simulations to be launched directly from the Project Navigator. All simulation commands that prepare the ISim simulation are generated by ISE Project Navigator and automatically run in the background when simulating a design using this flow. Adept is used for programming the board. The IP Cores for VGA and Ethernet are taken using Xilinx Vivado Design Suite.

4.2 ETHERNET INTERFACE

The on board 100MHz clock is divided to 25MHz and given to the PHY clock input. The 10BASE-T receiver gets the Manchester encoded analog signal from the RJ-45 cable via the magnetics. It recovers the received clock from the signal and uses this clock to recover the NRZI data stream. This 10M serial data is converted to 4-bit data nibbles which are passed to the controller via MII at a rate of 2.5MHz. The PHY IC receives the data from the Ethernet port and matches the destination IP with the IP of the device. Then the data is segregated and stored in memory. If the IP doesn't match, the packet is dropped. The UDP can support upto 1500 bytes of data payload in a single packet. But the FPGA is programmed in such a way that it accommodates 18 bytes of data. The entire size of UDP packet received along with 18 bytes of data payload is 72 bytes.

4.3 MEMORY INTERFACE

The memory interface is done through serial peripheral interface protocol. SPI is a synchronous serial communication protocol operating in full duplex mode. SPI communication pursues with master and slave modes of operation that is taken by devices considered. The master or slave designation is provided on the basis of preparatory part served by the device concerned. The above process is autonomous. Generally description of SPI protocol deals with four wires that specifies the data frame circulation. The four wires are MOSI (master out slave in), MISO (master in slave out), SS/CS (slave select/chip select), SCK (serial clock). It is always mandatory to generate clock thence the clock generator module has its maximum clock frequency to be reliant to the board. The venture prescribes the board to be Spartan-6 which has on board 100MHz clock. Thereby the clock is generated in such a way that to obligate frequency less than or equal to 100MHz. The process specifies that the data reads at the negative edge of the clock pulse given and writes at the positive edge of the clock. The positive and negative edges can otherwise be called as posedge and negedge or otherwise rising and falling edge. The above process can generally be called as the data encryption and decryption. In this venture the mandatory subroutine of reset condition is preliminarily tested are charted by escalation of count at binary levels. The above two statements will be common to both writing and reading process.

The reading phase of process has its preparatory part with an additional count initialized. This count accounts for the number of negative or falling edge that has been conceded. As stated above the subroutine of reset condition has been tested at the beginning. The variable accounting for the frontier of the data given has been initialized. This characterizes the maximum limit till the data decryption to occur. The decrypted data is stored in a new register initialized. As the frontier position reaches the termination is validated by the providing logic high. In concern at the rudimentary level after decryption of each data bit the next data's address variable is passed. The above process of decryption of data followed by passing address of the next one gives the analogy of algorithm for queue implemented with single linked list. Here the data decryption governs over the wire MISO, this exemplifies that the reading process is done by master with the data that the slave possess. In this venture the master signifies the commotion of UART and slave signifies the commotion of SPI memory device.

The writing phase has its preliminary part with the additional count as given for reading phase, this accounts for the number of positive or rising edges rather falling edges for reading phase that has been conceded. The same subroutine of reset condition is tested at the beginning. The variable governing the frontier of the data has been initialized. This characterizes the maximum limit to which the data encryption occurs. The encrypted data is shifted to the next address using shift register. The process of encryption of data in SPI gives the analogy of performing insertion operation in stack. The encryption governs with the wire MOSI, this exemplifies that the writing is done by master over the slave. In this venture the master signifies the activity of Ethernet and slave signifies the activity of the SPI memory device. Here an additional wire has been governed which is slave select, this wire chooses the appropriate SPI memory device i.e., a slave device.

4.4 UART INTERFACE

The UART is usually an individual integrated circuit used for serial communications over a computer or peripheral device serial port. UART provide flexibility to communicate with a wide variety of devices because the parameters are configurable. Common configuration parameters are Baud Rate, Stop Bit, Parity, Character Length (data bits), and Character Spacing. The UART is based on the two serial pins (RX & TX). In this module UART is implemented for recognizing the data received on the Ethernet. For the implementation of UART in FPGA the baud rate (baud rate is rate at which bits transfer) serves as the major factor. Baud rate is fixed by using clock divider method. The 100MHz clock present in our module is divided by the required baud rate of 9600bps provides the output of number of count i.e., 10416 count for a complete cycle .The obtained count value is converted for positive half cycle of the 100Mhz clock and then for every 5208 count the state changed from either 1 to 0 or 0 to 1. Thus the clock pulse of 9600bps is obtained. For every positive half cycle of the UART clock pulse the stored data undergoes an encapsulation of start (0) and stop (1) bits for every 8 bits of the 72 bytes Ethernet data received. The encapsulated data is transmitted by means of the transmitter pin (TX) of the bridge communication. Then the data transmitted undergoes an ASCII conversion and displayed in the terminal of the PC.

4.5 VGA INTERFACE

Video Graphics Array (VGA) refers specifically to the display hardware. The VGA converts the digital to analog signals to visualize the data to be customized in decisive to the reception concern, rather at the transmission level the activity is vice versa. In precise with the endeavor 10 signals are used for creating 8 bit colour resolution and 2 standard synchronization signals of horizontal and vertical traversing at the transmission level of VGA port in Nexys 3 board. The display is driven at 640×480 pixel resolution. The prescribed circuitry generally prevails with the current divider or resistor divider circuit with 75 ohms of termination. Thus each colour signal proceeds within the range of 0.0V to 0.7V with 256 different colour patterns.

VGA timing are specified, published and copyrighted by the company called VESA (Video Electronics Standards Association). Hence the architecture is named after this company. The physical link between the host and the display device taken is established using the DDC (Display Data Channel) protocol

devised by VESA. Rather at the elemental level, the nicety of the display device is provided using the EDID protocol (Extended Display Identification Data protocol).

The generalized timing formula is parameterized by Xfree86 Modline, which is a configuration file of the EDID to provide the information to the server about the display connected with the order of priority of resolution label, scanning type, horizontal and vertical synchronization of the display.

Here the horizontal and vertical scanning frequency is calculated by,

$$\text{Horizontal frequency} = pclk/h\text{-}total$$

$$\text{Vertical frequency} = pclk/h\text{-}total \times v\text{-}total$$

The scanning at transmission part is been done at interlaced level rather reception part is been proceeded with progressive level.

Hence the FPS (Frames per second) or in other words frame rate is as follows:

$$\text{FPS} = \text{field rate}/2 \text{ for progressive scanning}$$

$$\text{fps} = \text{field rate for interlaced scanning}$$

In this venture the EDID is automatically enacted and hence the reception part can be ignored. Transmission portrayal of the signals from FPGA is as follows.

On considering the customized data level, the video is thrown by the refreshing memory. The controller used here must accommodate in such a way that it must override the data transfer at the per pixel scanning time. Thence the synchronization pulses are enacted. This in precise deals with the pixel clock in response to the per pixel stimulation time in other words can be inferred as the response to each pixel with respect to the clock provided. The refreshing frequency is provided at the transmission level through vertical sync and retrace frequency is provided with the horizontal sync pulses.

To be specific the nexys-3 board operates at the frequency of 100MHz clock and the VGA port operates at the frequency of 25 - 30MHz clock. The on board clock is divided to 25MHz clock frequency and supplied to the VGA port. Here the clock division been conceded in such a way that the toggle of the respective pulse occurs at every 25ns on account of the frequency considered. Register Transfer Level (RTL) and bit level manipulations of configurations are considered in this work. The display is divided into 20×15 (300) blocks of size 32×32 pixels for accommodating 300 bytes of data. 640×480 resolutions consist of 307200 pixels and these tallies the partition of 20×15×32×32 which is 307200 pixels. The character set is written for 8×8 pixels which are later projected as 32×32 pixels.

A 16 bit register been initialized on account of projecting 8 bit colour resolution. The intervening registers are utilized for accessing through the memory required for the instantaneous endeavor. Finally pixel values been provided to activate the corresponding pixels for the customized data to be displayed. On considering the data box in other words called as LCD elemental division for particular character, is regarded for concatenated data with the separation of 8 bit as 4 + 4 bits from the MSB to LSB sequence. That is in precise to be needed for the box data traversing from left to right.

The synchronization between the displays in specific to be considered to have parameters like sync pulse, display time, pulse width, front porch and back porch. Horizontal and vertical timing sequence must be maintained till the penultimate level of the subroutine. Hence a 22 bit register been initialized for vertical timing sequence and 12 bit register is initialized for horizontal timing sequence. There by at the rudimentary level the preliminary reset condition is verified. Thence the vertical timing sequence reaches the threshold clock cycle of 416800 and then all the synchronization registers are kept low to receive data. As the vertical clock cycles reach the prior porch level (1600) vertical sync pulse is provided. Thence by now the vertical data reception is built ready for projection. Hence on perceiving at the horizontal process, as the clock cycle reaches the threshold value of 800 the registers meant for the horizontal synchronization is laid low for receiving horizontal pixel data. And finally as the recursive clock cycle reaches the value of 96 horizontal sync pulse is provided that accounts for the data packet completion which in turn ultimately to be projected to the display.

A VGA controller circuit decodes the output of a horizontal-sync counter driven by the pixel clock to generate HS signal timings. This counter can be used to locate any pixel location on a given row. Likewise, the output of a vertical-sync counter that increments with each HS pulse can be used to generate VS signal timings, and this counter can be used to locate any given row. These two continually running counters can be used to form an address into video RAM. No time relationship between the onset of the HS pulse and the onset of the VS pulse is specified, so the designer can arrange the counters to easily form video RAM addresses, or to minimize decoding logic for sync pulse generation. The character set is written as per the standard ASCII table where “A” is represented as 65 in hexadecimal. Similarly the remaining character sets are defined.

5. ZYNQ-7000 APSOC AS WEBSERVER

The Xilinx ZYNQ-7000 AP SoC is a new category of devices which combine an ARM dual-core Cortex-A9 MPCore processing system with advanced 28nm programmable logic. The range of devices in the ZYNQ-7000 All Programmable SoC family allows designers to target cost-sensitive as well as high-performance applications from a single platform using industry-standard tools. While each device in the ZYNQ-7000 family contains the same PS, the PL and I/O resources vary between the devices. Here a LAMP (Linux Apache MySQL PHP) server is built over Xilibus Operating system on ARM MPCore. The server possess SQL database which contains the information to be provided for the remote display device. Here the driver for VGA and Ethernet has been obtained using corresponding IPCores (Intellectual Property Cores).

6. RESULT ANALYSIS

The data from the remote PC is entered on a website which is a host of ZYNQ-7000(webserver). The entered data from the website is taken to SQL using PHP as a post request. The data from the post request is appended as a new row in the database table. The routine is made in such a way that as the data gets appended in the database, it is given to a specific web address or

IP address. This IP address or web address corresponds to the NEXYS 3 board which is attached to the display. In NEXYS 3 board the design entity is made in the form of Verilog HDL and a UCF file has to be created. A User Constraint File (UCF) is used to assign I/O pins in a design to the actual pins on the FPGA. The master UCF is available under NEXYS 3 board support package. The clock signal, SMSC Ethernet PHY, serial PCM memory and UART pins are mapped to the FPGA by adding the following parameters.

The design is simulated, followed by the generating the programming file, then the device is programmed using adept. The UDP data packet is sent from the server (ZYNQ-7000 APSOC). The FPGA receives the data, stores it in memory and then bypasses it to the UART port at 9600 baud rate. This communication port is monitored by a serial terminal application. The following Ethernet data was received by the FPGA,

55 55 55 55 55 55 55 D5 00 10 A4 7B EA 80 00 12 34 56 78 90 08 00 45 00 00 2E B3 FE 00 00 80 11 05 40 C0 A8 00 2C C0 A8 00 04 04 00 04 00 00 1A 2D E8 68 69 20 65 76 65 72 79 6f 6e 65 20 00 00 00 00 00 00 B3 31 88 1B

The received data is analyzed as follows

Ethernet preamble/SFD (synchronizer):

55 55 55 55 55 55 55 D5

Ethernet destination address: 00 10 A4 7B EA 80

Ethernet source address: 00 12 34 56 78 90

Ethernet type: 08 00 (=IP)

IP header: 45 00 00 2E B3 FE 00 00 80

IP protocol: 11 (=UDP)

IP checksum: 05 40

IP source (192.168.0.44): C0 A8 00 2C

IP destination (192.168.0.4): C0 A8 00 04

UPD source port (1024): 04 00

UPD destination port (1024): 04 00

UDP payload length (18): 00 1A

UPD checksum: 2D E8

UDP payload (18 bytes): 68 69 20 65 76 65 72 79 6f 6e 65 20 00 00 00 00 00 00

Ethernet checksum: B3 31 88 1B

The UDP payload data is of 18 bytes word length. The data is segregated from the packet and processed again as ASCII data, so that it can be viewed in Tera term, a serial terminal application as characters itself instead of hex values. The VGA character set for the corresponding data is written and displayed in a video graphics array display.

7. CONCLUSION AND FUTURE WORK

Thus the proposed system has been designed and implemented in Nexys 3 and ZYNQ-7000 APSOC. By adding the Internet of Things (IoT) application, the data has been directly fetched from a web page and displayed with much reduced latency. This enables automatic frequent update of Internet data to be displayed for applications like stock exchange, train schedules and any other public notifications. On further integration of APSOC with FPGA, can be a great revolution in modern computation system. This in turn provides much lower latency and very high performance with ultra-low power utilization.

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