DOI: 10.21917/ijme.2016.0050

AREA EFFICIENT, LOW QUIESCENT CURRENT AND LOW DROPOUT VOLTAGE REGULATOR USING 180nm CMOS TECHNOLOGY

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Abstract

This paper illustrates the design and implementation of a Low Drop out voltage regulator which consumes low power and occupies less area. The regulator uses single stage error amplifier hence area consuming compensation capacitor is avoided. It needs only 16μA quiescent current making it suitable for low power applications. The proposed regulator has been designed in 180nm CMOS technology and performance is tested using spice tool and layout is done using MAGIC VLSI tool. Simulation results show that the LDO has a line regulation of 0.001V/V and load regulation of 0.002V/mA. The LDO occupies an area of 70μm × 80μm and power dissipation is 20μW.

Keywords:

Linear Regulator, Low Drop-Out, Low Power, Power Management

1. INTRODUCTION

Power management is one of the dominant aspects of the modern integrated circuit design. The performance of any IC is heavily dependent on how the voltage is supplied and conditioned. Once line supply is rectified to a lower DC level, it has to be distributed to different sections of IC which needs different voltage levels. Also it has to be immune to line supply and load variations. In this regard, generally used components under power management scheme are linear regulators, switching regulators, reference voltage etc.

Though the efficiency of switching regulators is better than the linear regulator, they are more complex and noisier. In linear regulation, efficiency can be increased by adopting low drop-out [LDO] techniques. The Fig.1 shows typical architecture of a LDO.

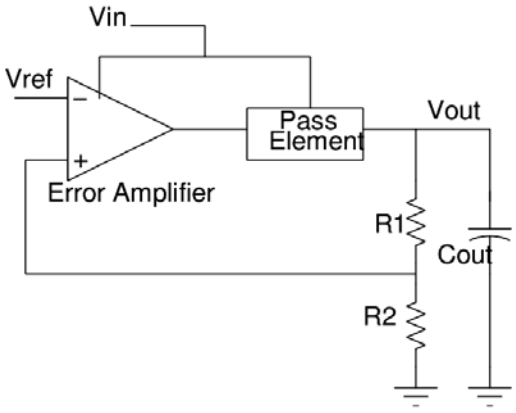

Fig.1. Typical Architecture of LDO

As shown in the Fig.1, error amplifier, pass element, feed-back network and external capacitor are the main blocks in LDO. The design of LDO starts with the design of pass element since it decides many vital performance parameters of LDO [1]. The pass element can be realized using Darlington pair, JFETs or MOSFETs. Among all MOSFET consumes less power and drop-out voltage can be made minimum. Also it can be integrated easily on a chip [2-4]. In MOSFET, either a PMOS in common source configuration or a NMOS in common collector can be used. However the latter produces a larger drop-out voltage. Hence a PMOS configuration is preferred. Once a pass element structure is decided, error amplifier has to be designed accordingly to drive the pass element and to perform corrective feed-back action. The line and load regulation of LDO mainly depend on the forward gain of error amplifier [5]. Error amplifier can be realized using different typologies like two stage, telescopic, folded cascode etc. However cascode is not suitable for low power applications, hence two stage is often used [6] [7]. One disadvantage in using two stage error amplifiers is the requirement of a compensation circuit which usually consists of a capacitor. Hence the complexity and area occupancy is increased [8].

The error amplifier needs a reference voltage which is temperature and supply voltage variation independent. Classic band gap reference cannot be used as it is unless modified to work below 1V [9], [10]. There are many techniques available for the same however at the cost of power, area and complexity. Usually output voltage is divided using resistors and fed back to error amplifier for comparison. The resistors must be large so as to reduce the quiescent current but it occupies a large area. The overall LDO needs a compensation scheme for stability purpose. There are mainly two approaches; either uses a large external capacitor in the range of micro farads or a small internal capacitor in the range of Pico farads which is integrated with the LDO. Both have merits and demerits. External capacitor improves the transient response considerably and makes LDO design simple but additional I/O pads must be provided. Whereas the second approach makes the system completely integrated however the transient response and stability are degraded. So additional circuits are required for the compensation which makes circuit design complicated and the power consumption is increased [11]-[15].

The section 2 describes the structure and design of the proposed LDO. The simulation results and Layout are presented in section 3 and results are analyzed and discussed. Conclusions are drawn in the final section.

2. DESIGN OF PROPOSED LDO

The aim of proposed design is to reduce the area occupancy, power consumption and complexity. So the Above mentioned aspects have been given the highest priority in selecting each component and building the architecture. The Table.1 shows the constraints and specifications considered for the design. The constraints suit for any battery operated low power applications.

Table.1. Constraints and Specifications of LDO

Parameter	Value
Technology	180 nm
V_{out}	1V
I_{max}	50mA
Quiescent Current	<15µA
Area	<100 µm X 100µm
V_{in}	1.3V
C_{out}	1µF

The design starts with pass element and a PMOS transistor is considered. The size of the PMOS depends on required drop-out voltage and maximum driving current. For the given specifications, 0.3V drop-out can be achieved by making W/L ratio of 11,111. Further reduction in drop-out voltage makes the size of transistor even larger and it occupies more space hence it is avoided.

While designing error amplifier, a simple and less power hungry topology is considered. A differential amplifier with active load as shown in Fig.2 meets the most of the specifications [14].

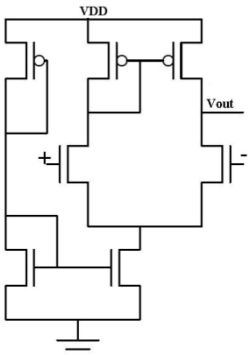

Fig.2. Differential Amplifier

The required output swing is decided by the gate voltage requirement of pass element. The variation of feed-back voltage determines input common mode voltage range of error amplifier. A suitable bias current is chosen so as to drive large pass element. Common mode voltage is taken as $V_{DD}/2$ i.e. 0.65V. Hence both reference voltage and feed-back voltage must be 0.65V.

Using resistor voltage divider, output is fed back to the error amplifier. Output 1V is divided into 0.35V and 0.65V using 35kΩ and 65kΩ respectively so as to feed 0.65V at the error amplifier input. Large resistors are chosen to reduce the quiescent current. The proposed LDO consumes 10µA quiescent current.

To reduce the chip area and complexity, the internal output capacitor is not used. To establish stability and have better transient response, an external 1µF output capacitor is used. The stability of LDO has to be analyzed properly since the system has feed-back and multiple stages. The number of poles, zeros and their location decides the stability. For system to be stable at least 45^0 phase margin is required [15]. The Fig.3 shows the small Signal model of proposed LDO.

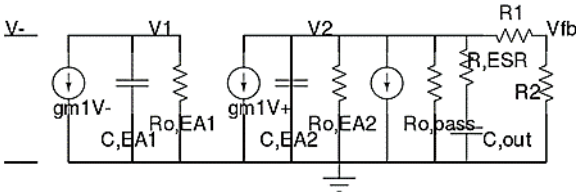

Fig.3. Small signal model of proposed LDO

The location of poles and zeros can be approximated as below,

$$f_{P1} = \frac{1}{2\pi C_{out} R_{o,pass} + R_{ESR}} \quad (1)$$

$$f_{P2} = \frac{1}{2\pi C_{EA1} R_{o,EA1}} \quad (2)$$

$$f_{P3} = \frac{1}{2\pi C_{EA2} R_{o,EA2}} \quad (3)$$

$$f_{Z1} = \frac{1}{2\pi C_{out} R_{ESR}} \quad (4)$$

where R_{ESR} is the effective series resistance [ESR] of output capacitor. Since system has 3 poles the stability is not guaranteed. However if any one of the pole is made dominant then phase margin can be greater than 45^0, stability can be achieved. Since a large output capacitor is used, the dominant pole lies at the output and it stabilizes the system. The Fig.4 shows the complete circuit diagram of proposed LDO.

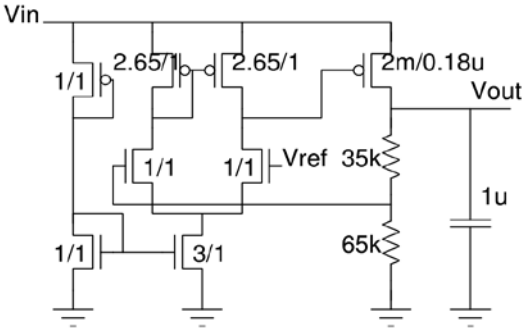

Fig.4. Circuit diagram of Proposed LDO

3. RESULTS AND DISCUSSION

The proposed design was simulated using LTspice tool and TSMC 180nm, SPICE model level=8 technology parameters. The Fig.5 shows the frequency response of differential amplifier. The open loop gain and unity gain bandwidth found to be 38 dB and 5MHz respectively.

The line regulation of LDO was tested by varying the input voltage from 1V to 5V and keeping the load current constant. The change in the output voltage was 3mV for entire range as shown in Fig.6. The load regulation was measured by varying the load current from 0 to 50mA. The output voltage varies only 10mV as shown in Fig.7.

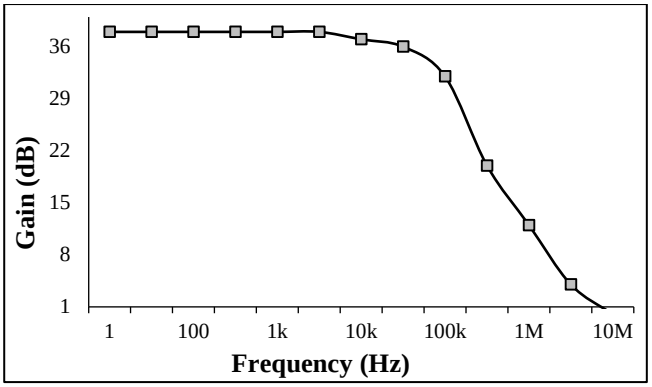

Fig.5. Frequency response of Differential Amplifier

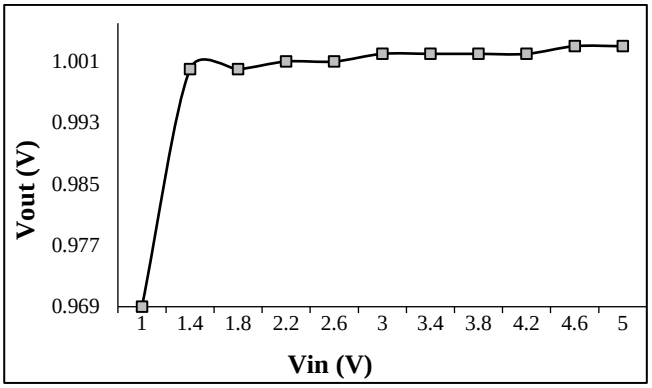

Fig.6. Line Regulation of proposed LDO

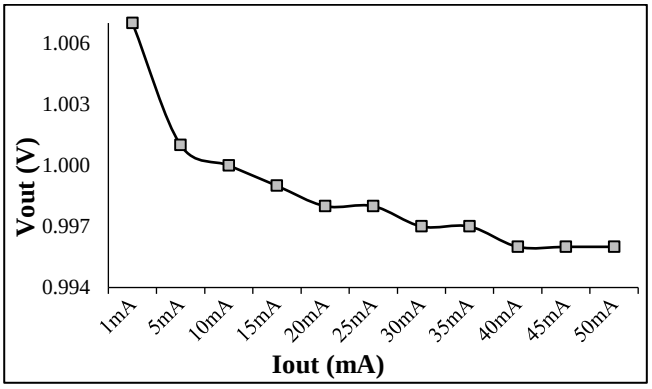

Fig.7. Load Regulation of proposed LDO

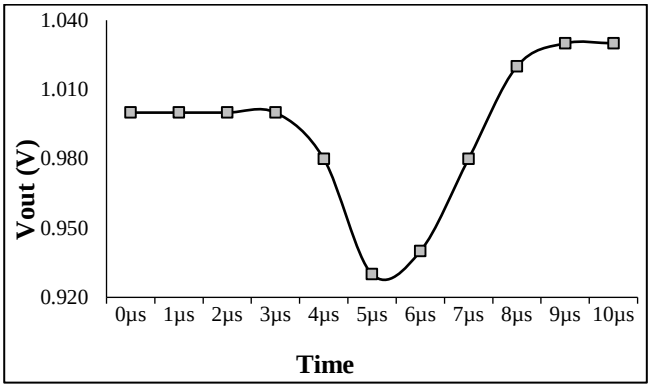

Fig.8. Load Transient Response of LDO

Load transient response of LDO was tested by applying a load pulse of 0 to 50mA with 1µs transition time, 4µs width after an initial delay of 3µs. A 70mV voltage variation was observed and LDO took 1µs to settle down as shown in Fig.8. Similarly a line voltage pulse of 0.2V was superimposed over 1.3V with 1µs transition time, 4µs width after an initial delay of 3µs. It was observed that there was an initial overshoot of 10mV and it settled down after 60µs as shown in Fig.9.

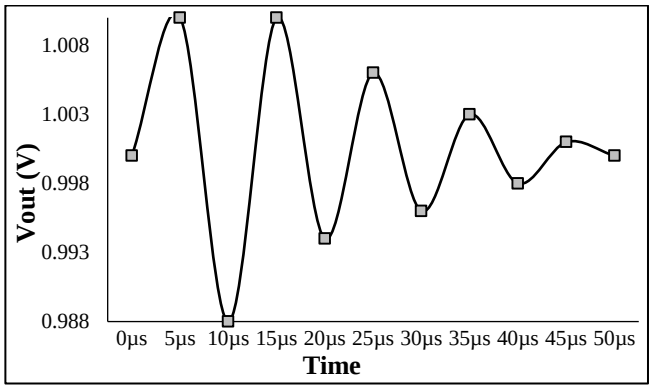

Fig.9. Line Transient response of LDO

Power Supply Rejection Ratio (PSRR) response of LDO was measured by applying an AC signal along with input DC voltage. The LDO showed 68dB gain (1/PSRR) at 1kHz, 21dB at 100kHz as shown in Fig.10.

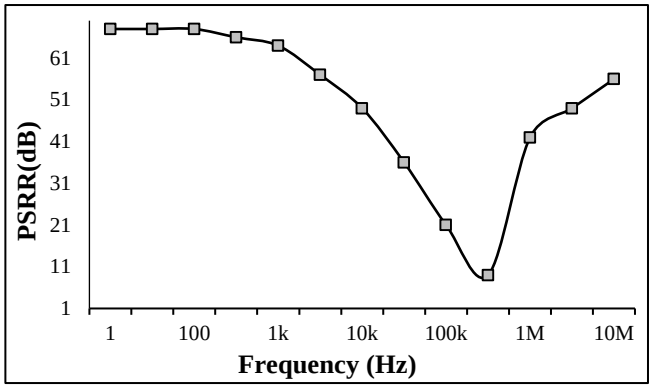

Fig.10. PSRR response of LDO

The proposed LDO was laid out in TSMC 180 nm MOSIS technology using MAGIC VLSI tool as shown in Fig.11.

The error amplifier used in proposed LDO is differential amplifier with the gain of 38dB. Though it is lesser compared to a two stage operational amplifier, it considerably reduces the area and quiescent current since compensation network is not needed. The line regulation and load regulation of LDO are mainly function of open loop gain of error amplifier. If two stage operational amplifiers had been used, the performance would have been a little better but at the cost of above mentioned parameters.

The dynamic parameters, load transient and line transient responses depend on the bandwidth of error amplifier, the parasitic gate capacitance of pass element, the output capacitor and maximum output current. The proposed error amplifier has unity gain bandwidth of 5MHz, the parasitic gate capacitance is approximately 1.5pF. The output external capacitor used is 1µF

hence measured transient responses are even comparable with complex, area and power hungry designs.

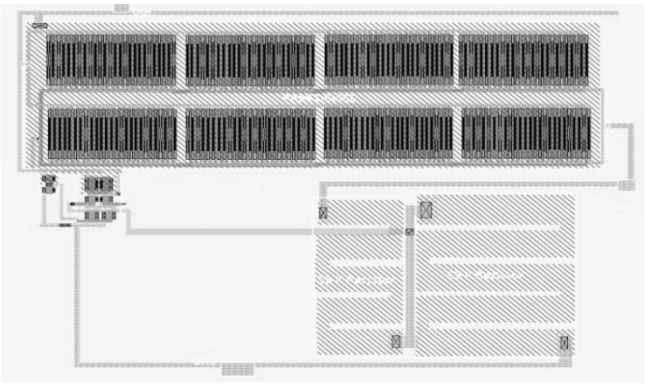

Fig.11. Layout of LDO

PSRR is the LDO's ability to reject any noise present in the input voltage. It varies with frequency of the noise. It is mainly dependent on control loop gain, external capacitor, ESR value of capacitor. The proposed LDO offers a decent PSRR response at all frequencies.

The key highlighting performance parameters of proposed LDO are drop out voltage, quiescent current and area occupancy. The dropout voltage is only 0.3V due to that the LDO offers high power efficiency. The error amplifier and feedback resistors consume 6µA and 10 µA quiescent currents respectively. Hence total quiescent current accounts to be only 16µA. The proposed LDO does not use any on chip capacitor; hence total area occupied is 70µm × 80µm.

The performance obtained from the proposed design is compared with the other recent works as shown in Table.2. It can be observed that proposed LDO performs better in area occupancy, quiescent current and drop-out voltage.

Table.2. Comparison of Proposed Design with Recent Works

Parameter	**[16]**	**[17]**	**[18]**	**[19]**	**Proposed Work**
Technology [µm]	0.35	0.35	0.18	0.18	0.18
$I_{out,max}$ [mA]	50	100	100	10	50
I_Q [µA]	26	25	61	50	16
ΔV_{out} [mV]	200	80	100	–	10
Settling Time [µs]	0.2	0.75	–	0.73	1
Drop-out [mV]	450	180	200	300	300
Area [mm^2]	0.098	0.126	–	0.005	0.005
C_L[F]	100p On-chip	100p On-chip	100p On-chip	–	1µ Off-chip

4. CONCLUSION

In this paper, challenges in designing a low drop out voltage regulator have been explained in detail. Further stability analysis of an LDO with external output capacitor has been carried out. An LDO with 1V output and capable of driving 50mA load current has been designed and laid out in 180nm CMOS technology. The proposed LDO consumes only 20µW power and occupies only 70µm × 80µm area with a drop-out voltage of 0.3V. This makes it highly suitable for low power battery operated device applications.

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