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PERFORMANCE IMPROVEMENT OF REVERSIBLE LOGIC ADDER

Richa Shukla[1] and Vandana Niranjan[2]
Department of Electronics and Communication Engineering, Indira Gandhi Delhi Technical University for Women, India
E-mail: [1]richa3090@gmail.com, [2]vandana7379@gmail.com

Abstract

Reversible logic is gaining importance in the context of upcoming fields such as nanotechnology, cellular automata, quantum level computation and low power VLSI design. The most attractive feature in reversible circuits is that there is one to one correspondence between input and output vectors. Therefore these circuits do not lose any information during computation. In this work we have improved the performance of reversible logic adder by modifying its structure. A delay and power efficient vedic multiplier has been implemented using proposed adder. All the circuits have been designed at 90 nm CMOS technology using Cadence Virtuoso software. Based on the results, it is concluded that the performance of a carry look ahead (CLA) adder gives best performance by changing the type of reversible gate used in its structure. The performance improvement is in terms of reduced number of gates by almost 60% reduced ancillary inputs by 46% and reduced number of garbage outputs by almost 48%. The proposed CLA adder may also find many applications in multiply and accumulate units.

Keywords:

Ancillary Inputs, Carry Look Ahead Adder, Garbage Outputs, Reversible Logic, Low Power

1. INTRODUCTION

With growing need for low power circuits new avenues have to be searched to eliminate any part of power consumed in the circuit or during its operation. Reversible logic implementation of classical circuits provides such an option. It all started with Rolf Landauer predicting a certain fixed amount of energy loss with every bit of information transfer [1], relating it to laws of thermodynamics, and Tomasso Toffoli suggesting that this amount of energy loss occurs only in irreversible or classical circuits and can be done away with by using reversible gates [2]. Reversible gates comply with one to one correspondence rule between inputs and outputs, which necessitates determination of input bit values from output obtained. There is no loss of bit during the computation. Therefore, such fixed energy loss does not occur in designs made from fully reversible gates.

The data path of any microprocessor consists of arithmetic circuits like adders, comparators, shifters which are in turn used in applications like multipliers and dividers. Binary adders are used in such data paths as all the computations done by a computer are in binary format. The way the carry is calculated in binary adders (by propagating, saving etc.) determines the delay in computation. Of course, the circuit complexity and area should not be significant. Therefore, efficient implementation of adders is an important issue in integrated circuit design.

In this work, the authors have improved the performance of one of the most widely used reversible logic adder. The performance in terms of number of gates, ancilla inputs and garbage outputs has been improved by modifying the internal structure. A comparison of the proposed adder with its conventional version validates the achieved performance improvements. Rest of the paper is organized as follows: Section 2 gives a brief background of reversible logic concept. In section 3, implementation of proposed adder has been reported. Vedic multiplier as application of proposed CLA adder is implemented in section 4. Results have been summarized in section 5 and section 6 concludes the work.

2. REVERSIBLE LOGIC CONCEPT

A well-formed reversible logic circuit is an acyclic combinational logic circuit in which all gates are reversible, and are interconnected without fan-out. So for a system to be reversible two conditions have to followed The first condition for any deterministic device to be reversible is that its input and output be uniquely retrievable from each other - then it is called logically reversible. The second condition: a device can actually run backwards - then it is called physically reversible. And the second law of thermodynamics guarantees that it dissipates no heat. While designing a circuit using reversible gates, it has to be kept in mind that output of previous stage does not drive more than one input of the next stage. For using an output more than once, the signal has to be replicated using any reversible gates. The gates are represented as black boxes which actually contain CMOS implementation of the functions obtained at the output, with equal number of inputs and outputs. The Fig.1 shows a general representation of a reversible gate.

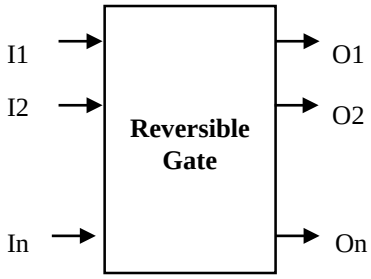

Fig.1. A reversible Gate

Since 1980 many developments have emerged in the field of reversible logic. A lot of useful reversible gates are available in literature such as Feynman gate [3], Toffoli Gate [4], Fredkin gate [5], Modified Toffoli gate [6], R gate [7] and double Peres gate [8]. Reversible gates are very useful in the nanotechnology and quantum computing regime. Ancillary inputs are those inputs which are maintained constant to realize a certain function from reversible gates. Garbage outputs are termed as those intermediary or final outputs which are not used further in the circuit. These are only the overheads which must be minimised in reversible logic based designs. In this work, the available reversible gates have been used to modify the existing adder structures to minimise the ancillary inputs and garbage outputs.

The core of every microprocessor, digital signal processor (DSP), and data processing application-specific integrated circuit (ASIC) is its data path. It is often the crucial circuit component if die area, power dissipation, and especially operation speed are of concern. At the heart of data-path and addressing units in turn are arithmetic units, such as comparators, adders, and multipliers [9]. Finally, the basic operation found in most arithmetic components is the binary addition. Besides of the simple addition of two numbers, adders are also used in more complex operations like multiplication and division. But also simpler operations like incrimination and magnitude comparison base on binary addition. Therefore, binary addition is the most important arithmetic operation. It is also a very critical one if implemented in hardware because it involves an expensive carry-propagation step, the evaluation time of which is dependent on the operand word length. The efficient implementation of the addition operation in an integrated circuit is a key problem in VLSI design. Addition is a prefix problem which means that each result bit is dependent on all input bits of equal or lower magnitude. Propagation of a carry signal from each bit position to all higher bit positions is necessary. Thus, carry bit is the primary concern for adder design.

3. PROPOSED ADDER

Different topologies of efficient reversible logic carry adders have been introduced [10-14]. Carry look ahead (CLA) adder is a faster addition option as it calculates one or more bits of carry ahead of sum value so that time is saved while calculating values containing larger bit. CLA adder is based on the theory of calculating carry out in terms of carry in only , and is not dependent on the previous values of carry. For this to happen, generate and propagate bits are calculated first, as per the equations given below,

$$G_i = A_i.B_i \quad (1)$$

$$P_i = A_i \oplus B_i \quad (2)$$

$$C_{i+1} = G_i + P_i.C_i \quad (3)$$

$$S_i = P_i \oplus C_i \quad (4)$$

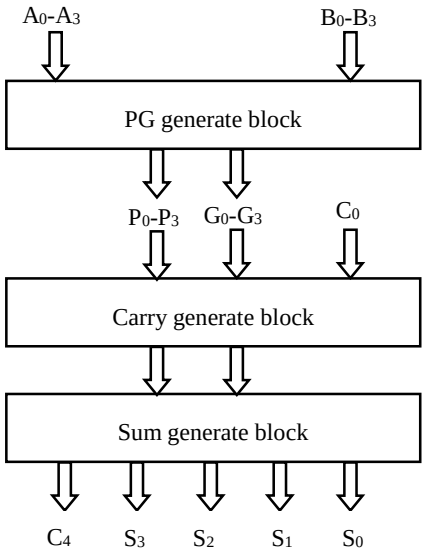

Fig.2. Carry look ahead adder working principle

where, *P*, *G*, *C*, *S* stand for generate, propagate, carry and sum respectively with subscript denoting bit value. We can easily see that carry of last stage would be-

$$C_4 = g_3 + p_3.g_2 + p_3.p_2.g_1 + p_3p_2.p_1.g_0 + p_3p_2.p_1.p_0.C_0 \quad (5)$$

Hence, carry dependence of previous stage is eliminated. The Fig.2 shows the working principle of CLA adder.

In [10], a 16 bit adder is designed by cascading 4 bit CLA adders. The 4 bit CLA adders are made up of:

1) *P* and *G* generate block - using 4 Feynman gates and 4 Toffoli gates
2) Carry generate block using 10 Feynman and 20 Toffoli gates
3) Sum generate block using 4 Feynman gate.

So, in total number of gates are 42 with quantum cost of 138. Such numbers ensures increased ancillary and garbage figures also. Although this structure uses basic gates only but suffers from high quantum cost and number of gates and hence greater ancilla and garbage overheads.

The proposed CLA adder is shown in Fig.3. In the proposed structure, *P* and *G* blocks are implemented using *R* gate and carry generate block is designed using Toffoli and Modified Toffoli gates. Sum generate block is designed using Feyman gate and is same as that in conventional CLA structure. This has led to significant reduction in number of gates and improvement in other parameters.

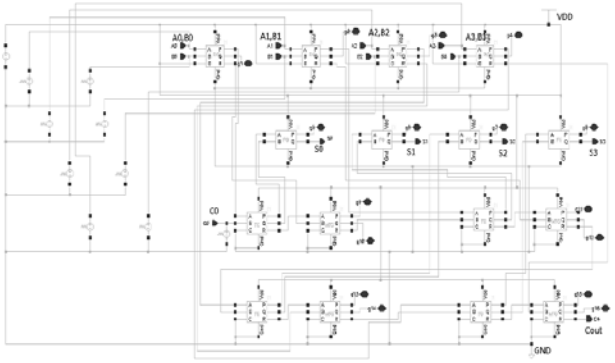

Fig.3. Proposed Carry Look Ahead Adder

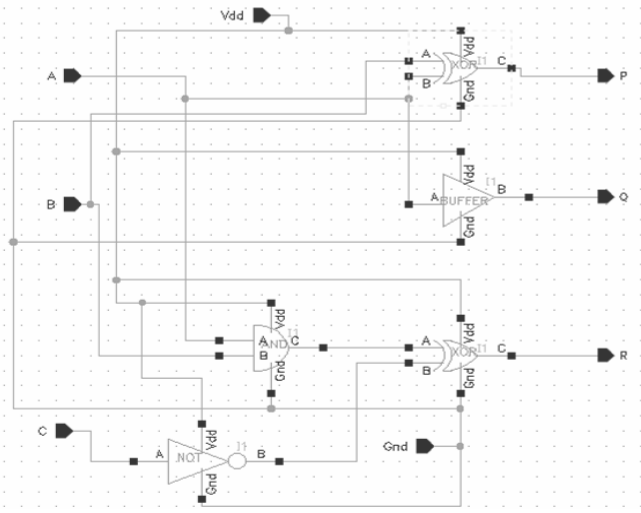

Fig.4. Schematic of R gate

The Fig.4 shows schematic of *R* gate, which uses 2 XOR, a NOT, a BUFFER and a AND gate. The Buffer used in Fig.4, is implemented as shown in Fig.5 using 2 NOT gates. In turn the NOT gates are implemented on transistor level as in Fig.6.

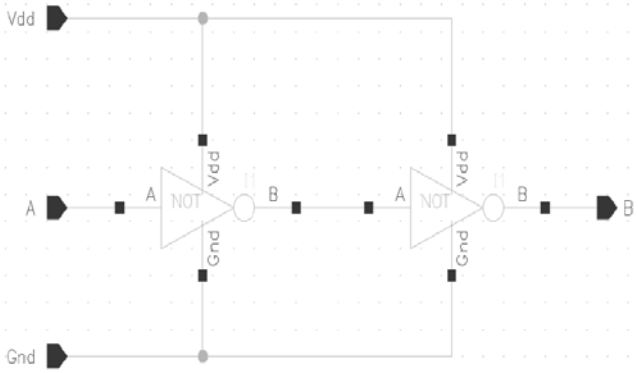

Fig.5. Schematic of buffer

The schematic of Feynman gate used in proposed CLA adder is shown in Fig.7. The XOR gate in the Feynman gate is made using NAND shown in Fig.8. The buffer in Feynman gate is same as in Fig.5.

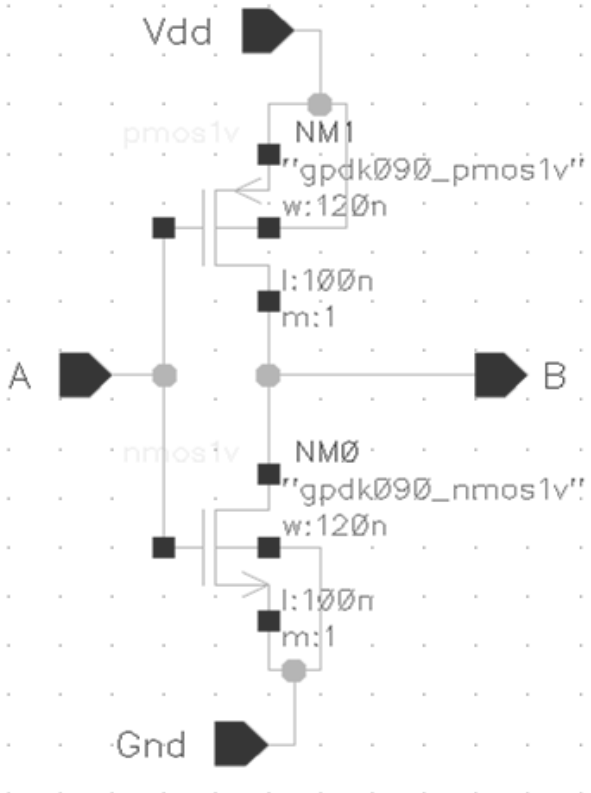

Fig.6. Transistor implementation of inverter

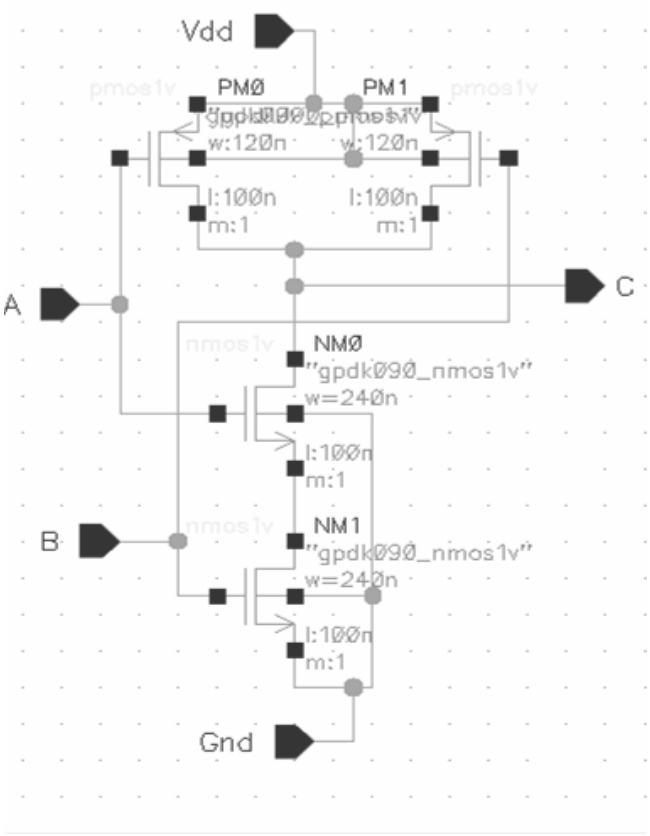

Fig.7. Schematic of Feynman gate

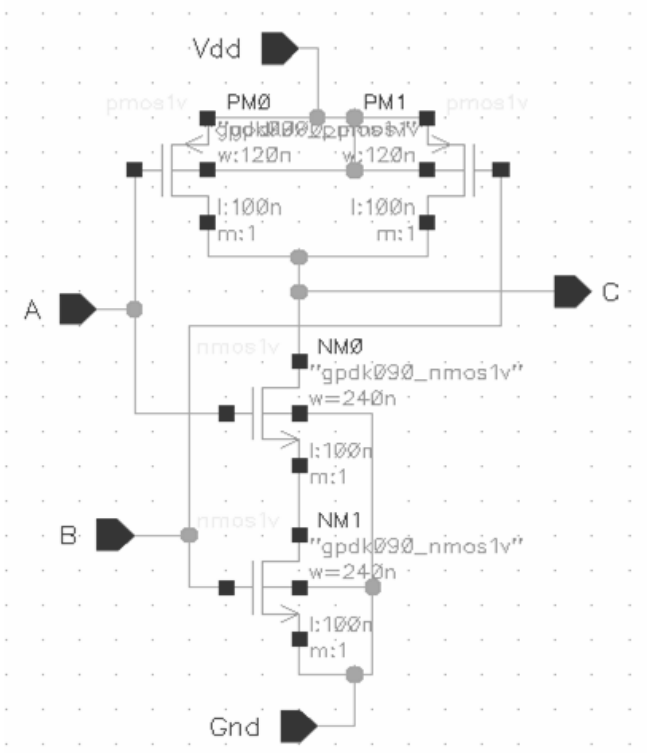

Fig.8. Transistor implementation of NAND gate

The Fredkin gate and Modified Toffoli gates used in proposed CLA adder are shown in Fig.9 and Fig.10 respectively

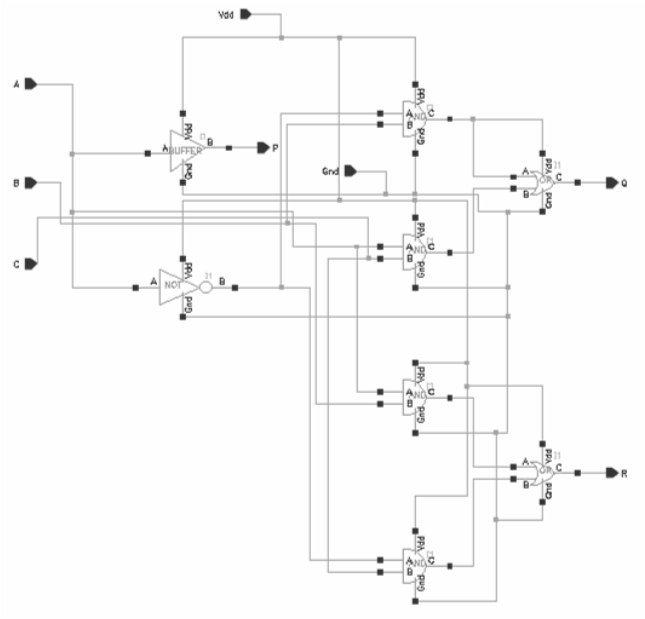

Fig.9. Schematic of Fredkin gate

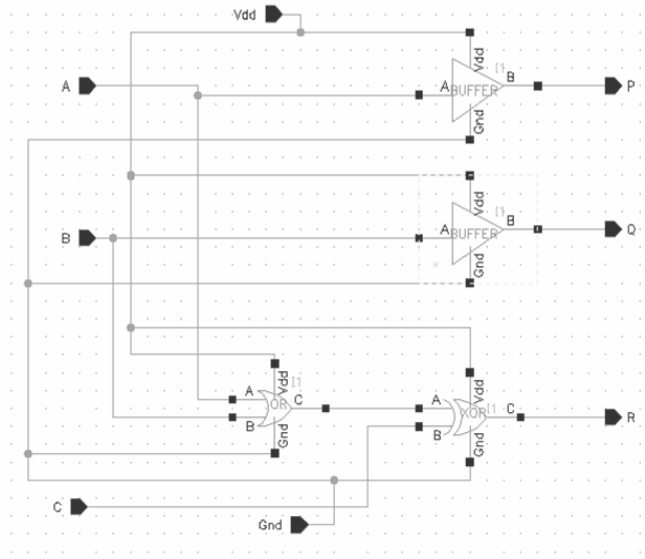

Fig.10. Schematic of Modified Toffoli gate

4. APPLICATION OF PROPOSED CARRY LOOK AHEAD ADDER

With evolving technologies, faster operations like addition and multiplications are need of the hour. Higher frequency of operation demands faster arithmetic operations. Multiplication stands critical in determining the speed of the CPU. Multiplication involves partial product generation and their addition, hence is a time consuming process. It is therefore, required that this process be simplified as much as possible. Doing so will further help in applications like convolution, Discrete Fourier Transform, Fast Fourier Transforms, etc for which multiplication forms the basis.

Many algorithms for multiplication have been proposed over the time and each has their own characteristics. Vedic Mathematics offer one such simple and efficient way of multiplying two numbers. It is especially beneficial for addition of large bit numbers as all complex multiplication is broken down into simple steps which can easily be calculated in mind .It is one of the most ancient methodologies used by the Aryans. One major problem with other algorithms for multiplication is that as the number of bits increase, the associated time delay increases in the same proportion. This is not the case with the Urdhva Tiryakbhayam algorithm. Hence one can limit the clock frequency to a lower value. Also, since processors using lower clock frequency dissipate lower energy, it is economical in terms of power factor to use low frequency processors employing fast algorithms [15].

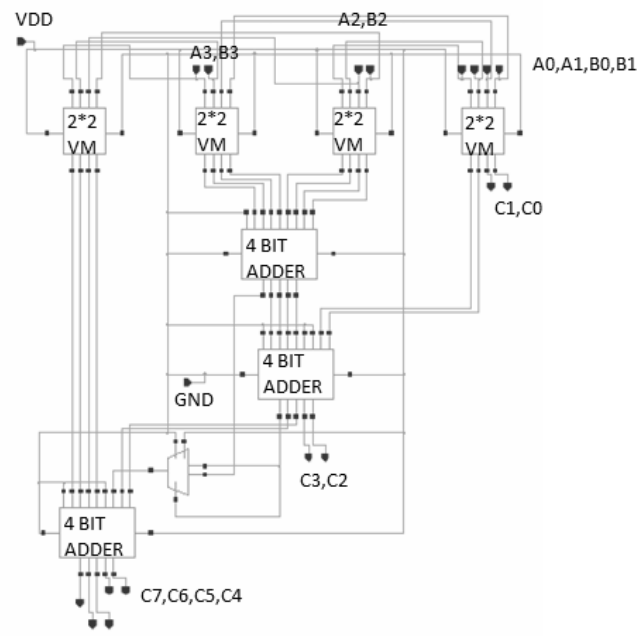

Fig.11. Proposed 4×4 Urdhva Triyakbhayam Vedic Multiplier

The proposed Urdhava Triyakbhayam Vedic Multiplier is shown in Fig.11. This multiplier may find use in Fast Fourier Transform filters, in DSP like imaging, software defined ratios and wireless communications. This Multiplier has the advantage that as the number of bits increases, gate delay and area increases at a slow pace as compared to other conventional multipliers. The upper four blocks are 2×2 Vedic multipliers, lower ones are three proposed carry look ahead adder and a multiplexer.

The first two digits of first 2×2 vedic multiplier form the LSB's of the multiplication result (C_0 and C_1). Next, the results of second and third 2×2 vedic multipliers are added using the proposed carry look ahead adder. The MSB of the result serves as a input to the multiplexer, while the rest of the bits are added with the remaining bits of first 2×2 vedic multiplier. Again the first two bits of this addition serve as the third and fourth bits of the final result (C_2 and C_3). The rest of the digits are passed on for next addition leaving the MSB, which serves as multiplexer input and control line simultaneously. Depending on its value either the MSB from first adder or the second is selected. This value is passed on for final addition as carry. Last adder takes this carry, the output of fourth 2×2 vedic multiplier and remaining bits of second adder as inputs and produce remaining bits of the final result (C_4 - C_7).

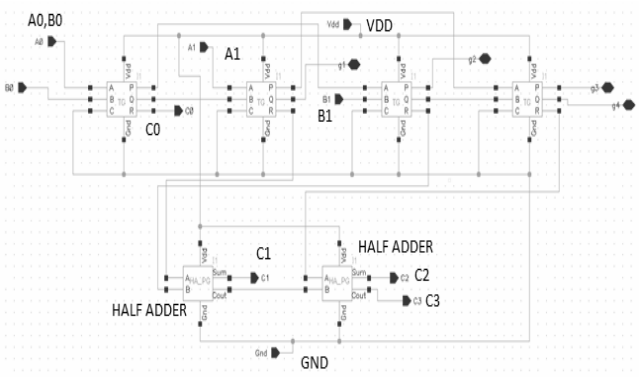

Fig.12. Proposed 2×2 Vedic Multiplier

The Fig.12 gives the implementation of 2×2 multiplier. The Tofolli gates serve to perform AND operation and the two 2 bit adders add the partial products. The half adders in Fig.12 are implemented using Peres gate as shown in Fig.13 whereas multiplexor is implemented using Fredkin gates as shown in Fig.14. This is the simplest reversible implementation of multiplexer. The four bits of 2×2 vedic multiplication are obtained as A_0 AND B_0 gives LSB (C_0) from the Toffoli gate. C_1 from first half adder whose carry goes to next half adder to give C_2 and C_3.

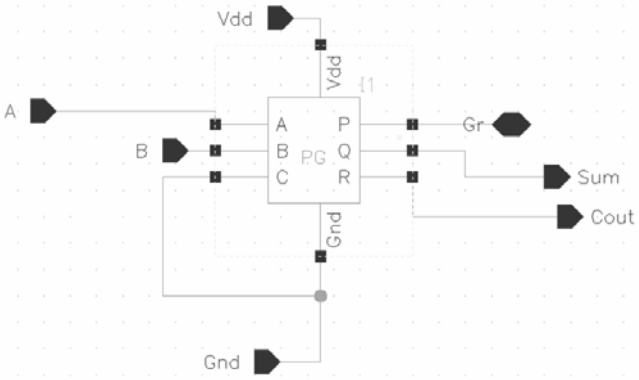

Fig.13. Half adder using Peres gate

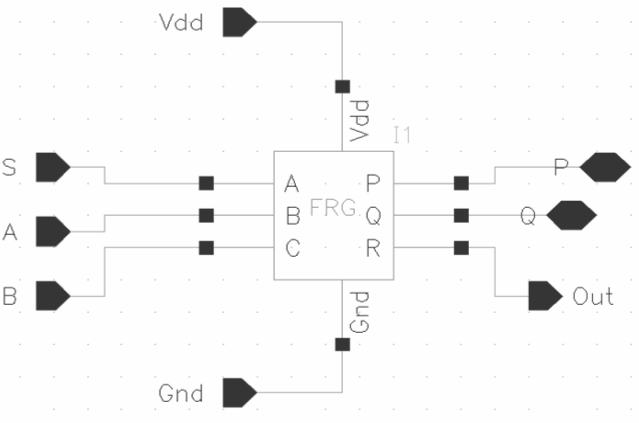

Fig.14. Schematic of 2×1 MUX

5. RESULTS

Simulations of all the circuits were performed in Cadence Virtuoso using 90 nm CMOS technology at supply voltage of 2V. The proposed adder has been compared with conventional version in Table.1. The Fig.15 shows the results for CLA adder.

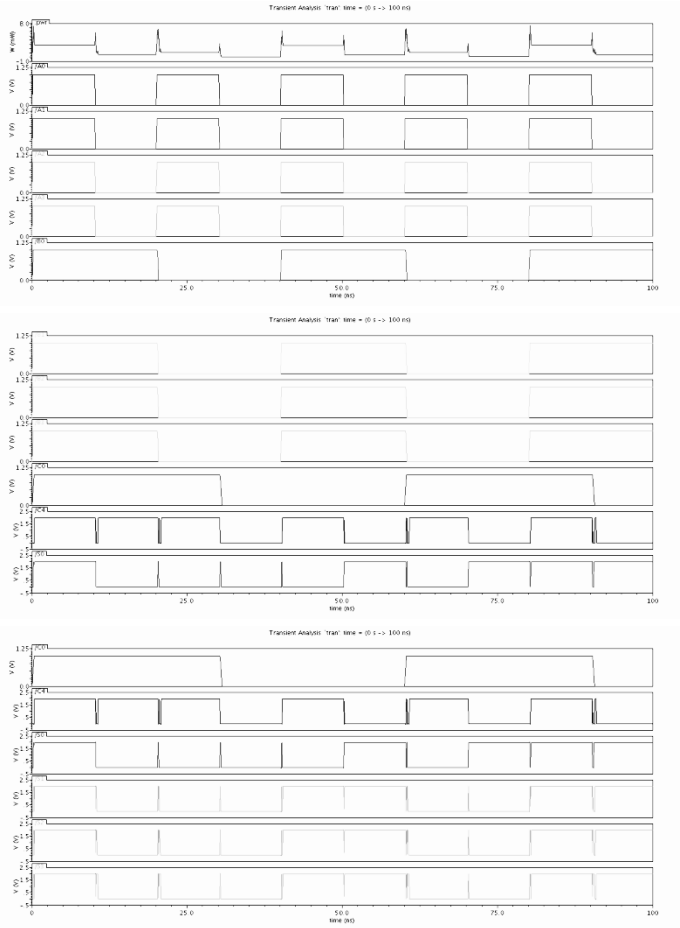

Fig.15. Simulation results of proposed reversible CLA Adder

Table.1. Comparison of Proposed CLA adder with conventional adder

Parameter	Conventional CLA adder [10]	Proposed CLA adder	Percentage improvement
Number of Gates	42	16	61.9
Ancillary input	30	12	46.6
Garbage outputs	31	16	48.3

From Table.1 it is observed that a significant improvement is obtained in all three parameters in the proposed CLA adder. Simulation results of 4×4 Vedic multiplier are shown in Fig.16. The Table.2 summarizes the results for 2×2 vedic multiplier and Table.3 summarizes the results for 4×4 vedic multiplier.

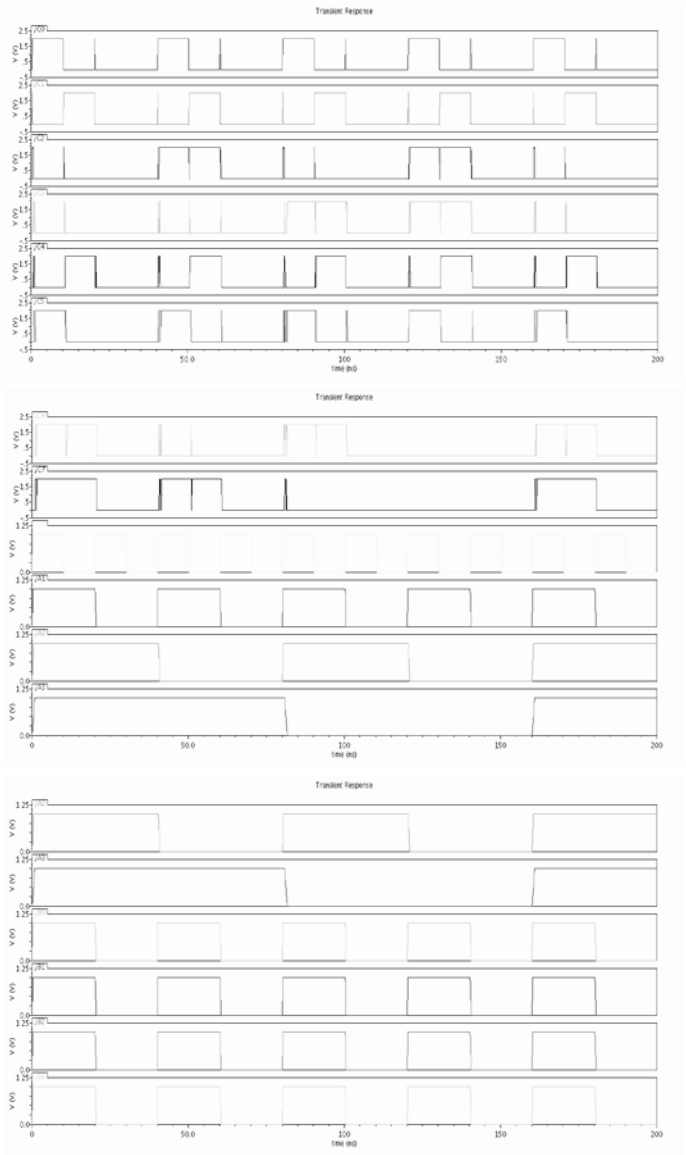

Fig.16. Simulation results for proposed 4×4 vedic multiplier

Table.2. Simulated results of 2×2 vedic multiplier

Power Dissipation	467.1uW
Delay C_3	176.9ps
Delay C_4	169.5ps

Table.3. Simulated results of 4×4 vedic multiplier

Power Dissipation	2.254mW
Delay C_7	431.9ps
Delay C_6	636.6ps
Ancilla inputs	60
Garbage outputs	74

6. CONCLUSION

Reversible Logic provides good option for low power VLSI design-helpful in eliminating power dissipation per computation. Also, reversible logic circuits act as fault tolerant circuits when made with certain reversible gates. There is a vast scope of applications in nanotechnology and quantum computing. The paper presents a new reversible logic implementation of carry look ahead adder. The adder is efficient in terms of parameters such as garbage outputs, ancilla inputs and quantum cost. A vedic multiplier has been implemented using proposed adder. The proposed vedic multiplier structure is both power and delay efficient and can be used further in areas of signals and systems and digital signal processing.

The designs are optimum in terms of the parameters discussed; the improvement can be achieved with discovery of new reversible logic gates that offer reduction in quantum cost. There is a need to research and identify the gates which result in reduction of redundant parameters when used in a particular design.

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